Emulation of a Navigation Processor with Physical Memristors Models

Karlheinz Ochs, Enver Solan, Dennis Michaelis, and Leonard Hilgers

Ruhr-University Bochum
Chair of Digital Communication Systems
Bochum, Germany
Email: {karlheinz.ochs, enver.solan, dennis.michaelis, leonard.hilgers}@rub.de

***Index Terms*—Memristive networks, self-organization, emulation, shortest path.**

***Abstract*—Self-organizing circuits are subject to current research with the respect to machine learning in which memristors are the essential devices to enable the desired functionalities. Since the inherent nature of a current is to flow along the path of least resistance, circuit-inspired solutions are good candidates to solve the problem of finding the shortest path through a maze. While this navigation problem has been realized with theoretical models of memristors before, it has not been addressed by using real memristors. The goal of this paper is to employ a physical model of a real HfO_2-based RRAM memristive device to create a real navigation processor. We utilize the wave digital concept as an emulation technique to create a circuit-inspired navigation processor with underlying models of real memristors. We therefore provide the necessary tools for future hardware realizations of self-organizing circuits in this work.**

I. Introduction

With the aspect of making machine learning possible, self-organizing circuits are of particular interested in current research [1]. Due to the inherent massive parallelism of voltage and current, these circuits enable potential efficient solutions to mathematically complex problems. One of these problems is a navigations processor that essentially aim to find the shortest path between to nodes, which can be interpreted like finding the shortest path from an entry node to an exit node in a maze [2]. The here exploited analog parallelism makes circuit solutions superior to all existing graph theoretical algorithms, as they solve the shortest path problem in only a single step.

Inspired by the concept of solving a maze by a memristive circuit in [3], we extend the approach by utilizing a physical memristor model to verify the proper functioning in a circuit with memristors that have been manufactured recently [4]. In general, memristors are the essential devices to facilitate the desired functionalities in such circuits [5]. Resistive random access memory cells (RRAM-cells) are common in memory applications [6], [7], but since their interpretation as memristive devices they became popular in self-organizing circuits [8]. Recent results have led to a deep understanding in filament growth and switching behavior of HfO_2-based RRAM-cells, which are popular in time-critical applications due to their fast transition between high and low resistance state [9].

However, as real memristive devices in general are not well examined and the manufacturing process is costly, emulators based on operational amplifiers are often used to aid the development process for memristive devices [10], [11]. A major drawback of this approach is that the amplifiers are active elements and the stability of the resulting overall setup can in general not be guaranteed.

An approach to overcome these restrictions is the wave digital method [12], which has successfully been used to emulate memristors while preserving passivity [13]–[15]. This approach yields a massively parallel algorithm which can be implemented on a digital signal processor (DSP) or a field programmable gate array (FPGA) to emulate RRAM-cells embedded in an analog circuit. An additional benefit is that parameters can be changed during runtime, allowing for live parameter optimization and live sensitivity analysis.

The paper is structured as follows. In Sec. II details on the deployed RRAM-cell is presented and the circuit of the navigation processor is derived. The wave digital model of this circuit is then established in Sec. II-D, and a proper functioning is verified through the emulation results in III. A final conclusion summarizes the main results.

II. Methodology

A. General Circuit Design

The goal of a navigation processor is to find the shortest path between two points. One possible way to interpret this task is to think of it as a maze where the goal is to find the shortest way to the exit. Fig. 1 shows such a maze and the underlying electrical circuit that is assumed throughout this work. An electrical interpretation of the search for the shortest path is reasonable because a current inherently guides its way through the path of least resistance in an electrical circuit. So by applying a proper voltage u between the nodes, the current i will naturally find the shortest path from one node to the other.

The interconnection between the nodes and how to design these are discussed in the following. The solution presented in this work is based on real RRAM-cells, showing that the problem can be solved with real memristive devices.

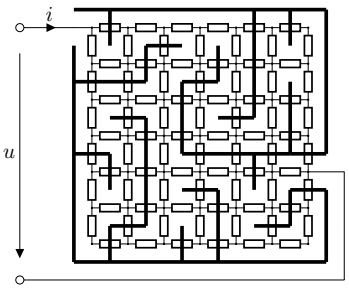

Fig. 1. A 7x7 maze with the goal to find the shortest path from entry to exit and the underlying structure of its general electrical interpretation of the problem through a circuit consisting of nodes and connection elements as in [2].

B. RRAM-Cell

The here deployed RRAM-cell is a HfO_2-based, voltage controlled memristor which was established in [9], see Fig. 2. Its modeling is practical and facilitates investigations with real memristors. The low resistance state can be described by

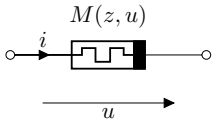

Fig. 2. RRAM-cell as a memristive one port.

$$R_0 = \frac{1}{NG_\mathrm{q}}, \text{ and } G_\mathrm{q} = \frac{i_0}{u_0}, \tag{1}$$

where N is the number of conducting paths through the memristive layer and G_q, i_0, u_0 are normalization constants with the physical units of a conductance, current and voltage, respectively. The high resistance state is

$$R_1(u) = \frac{u}{G_\mathrm{q}u + i_0 \ln\left(\frac{1+e^{\gamma-\beta u/u_0}}{1+e^{\gamma+[1-\beta]u/u_0}}\right)}, \tag{2}$$

where γ describes the gap between conducting filaments and β the voltage division ration between pre and post potential barrier.

The voltage current relationship reads

$$\begin{aligned} u(t) &= M(z,u)\ i(t), \\ M(z,u) &= R_0 + z[R_1(u) - R_0], \end{aligned} \tag{3}$$

where $M(z,u)$ is the memristance and it is noted that $z = 0$ describes the RRAM-cell in the low resistance state, whereas $z = 1$ refers to the high resistance state. The state equation to describe the inner state z is given by

$$\begin{aligned} \dot{z} &= g(u)[\sigma(u)\sigma(z) + \sigma(-u)\sigma(1-z)], \\ g(u) &= S_\mathrm{p}\Sigma(u - U_\mathrm{tp}) + S_\mathrm{n}\Sigma(u - U_\mathrm{tn}), \end{aligned} \tag{4}$$

where $\sigma(\xi)$ is the Heaviside function, $\Sigma(\xi) = \int_0^\xi \sigma(\eta)\mathrm{d}\eta$, S_p and S_n describe the steepness of transitioning from R_1 to R_0 and vice versa, respectively, and U_tn and U_tp are the negative and positive thresholds for the transitional behavior, respectively.

C. Connection Element

The connection element shown in Fig. 1 is described the setup in Fig. 3 which deploys the RRAM-cell describes in Sec. II-B. It consists of an anti-parallel connection of two RRAM-cells M_1, M_2 and two switches S_1, S_2. The anti-parallel connection of two RRAM-cells is necessary since memristors in general are direction-dependent. The initial states of both memristors is the high resistance state and if this connection element is part of the shortest path, the according memristor will switch to the low resistance state. The task of switches S_1, S_2 then is that the states of the switches determine if a connection can be used in both or only a single direction. This enables the setup to solve directed and undirected graphs alike.

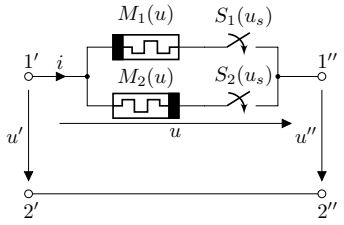

Fig. 3. Connection element consisting of an anti-parallel interconnection of two RRAM-cells M_1, M_2, and two switches S_1, S_2 with their states depending in the sensor input u_s to model obstacles, eg. walls, and to enable unidirectional paths.

The second purpose of the switches is to represent obstacles like walls in a maze, in which case both S_1 and S_2 would be in the open state so that no current can flow. This is determined by a sensor signal u_s, where one possible realization could be the projection of the maze topology through light where bright areas indicate a way and dark areas indicate obstacles, so that the appropriate sensor voltage u_s can be obtained by a light sensor.

D. Emulation Concept

The wave digital emulation model of the here deployed RRAM-cell was discussed in detail in [16]. Due to lack of space we only briefly highlight the most relevant features. The wave digital algorithm [12] involves a discretization that will translate differential equations into difference equations through numerical integration. A popular choice for the integration method is the trapezoidal rule, because it is known to be the most accurate passive linear multistep method [17]. For example, the numerical integration of a capacitance leads to

$$u(t_k) \approx u(t_{k-1}) + \frac{T}{2C}[i(t_k) + i(t_{k-1})], \tag{5}$$

with equidistant instances t_k and sampling period T. By introducing the voltage waves a, b and the port resistance R,

$$\begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} 1 & R \\ 1 & -R \end{bmatrix} \begin{bmatrix} u \\ i \end{bmatrix}, \quad \text{with } R > 0, \tag{6}$$

the implicit relation in (5) becomes explicit

$$b(t_k) = \frac{T}{2C} a(t_{k-1}).$$

This results in tremendous advantage in real time requirements.

In this work, a wave representation of a memristor is of interest. In general, a resistor is described by

$$u = R_0 i \quad \overset{(6)}{\Leftrightarrow} \quad b = \frac{R_0 - R}{R_0 + R} a = \rho a,$$

where ρ is the reflection coefficient. In the case of a memristor, this reflection coefficient has a memory.

III. Results

A. RRAM-Cell and Connection Element

RRAM-cell parameters			
i_0	38.74 μA	R_0	10 kΩ
u_0	0.5 V	S_p	-50 Hz/V
N	1.5	S_n	-0.4 Hz/V
β	0.1	U_tp	1 V
γ	3.8	U_tn	-0.5 V

TABLE I
PARAMETERS FOR THE RRAM-CELL (1)-(4).

The hysteresis curve of the single RRAM-cell, see Fig. 2, with parameters as in Table I is shown in Fig. 4 (left). The typical fast switching behavior of the cell can be observed around $u = U_\mathrm{tp}$, and it is key to the fast convergence of the circuit. The hysteresis curve of the connection element in Fig.

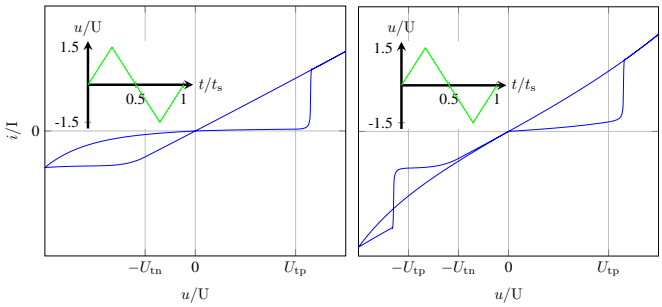

Fig. 4. Hysteresis curves given the triangle inputs displayed in the top corners of the single RRAM-cell of Fig. 2 (left) and the connection element of Fig. 3 (right).

3 is shown in Fig. 4 (right). The resetting process which can be observed around $u = -U_\mathrm{tn}$ and $u = -U_\mathrm{tp}$ is essential if the topology of the maze changes during runtime and a previously optimal path is now blocked through a wall. In that case the circuit itself should transfer that particular connection element from a low resistance state to a high resistance state, emphasizing the aspect of self-organization.

B. Navigation Processor

We investigate four different scenarios of mazes to obtain insights on the proper functionality of the RRAM-cells in the setup. The results are shown in Fig. 5. In the first scenario, which is shown in the far left column of Fig. 5, discusses the maze depicted in Fig. 1. The shortest path, indicated by the red line, is found after approximately $t = 0.25\ s$. This can be observed from the course of the current, since once all memristors along the path are in the low resistance state, the current will achieve its maximum value. In the following, this scenario will be used as a reference to which we will compare the three upcoming scenarios.

The middle left column of Fig. 5 reveals the behavior of our approach in a significantly bigger 20x20 maze which has over 8-times more nodes than the 7x7 reference maze. It is worth noting that the convergence time with $t \approx 18\ s$ is even lower than in the reference scenario which is due to the fact that a higher voltage between entry node and exit node has to be applied in order for the RRAM-cells to switch. So technically, the convergence time is only restricted by the speed in which the deployed memristive device can switch from high resistance state to low resistance state. The important feature is that all memristive devices along the shortest path will switch simultaneously at the same time, highlighting the massive parallelism of electrical circuits and explaining why the size of the circuit has no effect on the convergence time.

A maze with two equally long shortest paths is investigated in the scenario shown in the middle right column of Fig. 5. At $t = 0.25$ s both of these paths are found, indicating that having multiple optimal paths does not affect the convergence time. By taking the stochastic nature of RRAM-cells into account, it is to expect that only one of two equivalently long paths would be found, depending on which cells switch first.

The fourth and last scenario of interest is shown on the far right column of Fig. 5 and highlights the self-organizing aspect of the circuit. The initial shortest path is found after $t < 0.1$ s, yet at $t = 0.38$ s an obstacle close to the exit node is blocking the previously optimal path. In around 0.02 s the newly shortest path is found, indicating that the approach is highly adaptable during runtime, dynamical and self-organizing.

It is to be stressed that the topology seems a negligible influence on the speed of convergence. Therefore, properly designed memristive circuits are justifiable candidates to solve problems that would take excessive runtimes through sequential processing.

C. Runtime

Runtime Comparisons		
Scenario	LTspice	Wave Digital
1	208 s	0.645 s
2	200 s	0.657 s
3	189 s	0.661 s
4	192 s	0.654 s

TABLE II
RUNTIME COMPARISONS OF THE FOUR SCENARIOS IN FIG. 5 (LEFT TO RIGHT), REVEALING A CLEAR ADVANTAGE OF THE WAVE DIGITAL ALGORITHM COMPARED TO THE LTSPICE SIMULATION.

Table II gives an overview over the runtimes required by implementing the underlying circuits of the scenarios in Fig. 5 as an LTspice simulation and a wave digital model. Because of the reasons explained in Sec. II-D, these results confirm a highly significant runtime advantage by deploying

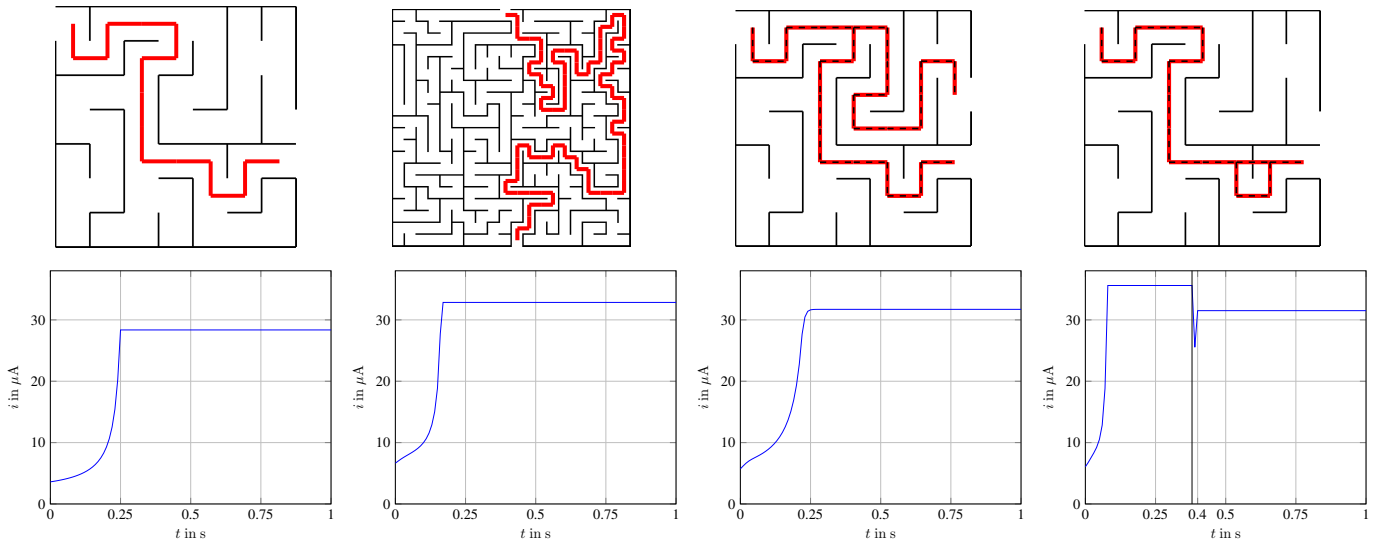

Fig. 5. Simulation results of the four investigated scenarios with the top row showing the topologies of the mazes and the bottom row depicting the behavior of the respective current. The scenarios are the small 7x7 maze of Fig. 1 as the reference (far left), a bigger 20x20 maze to show the excellent scalability (middle left), a maze with two equally long optimal shortest paths which are both found when non-stochastic RRAM-cells are deployed (middle right) and an added obstacle at $t = 0.38\ s$ to the previously optimal path to prove the self-organizing nature of the setup (far right).

the wave digital algorithm. Additionally, we had to deploy a simplified model of the RRAM-cell under LTspice, since the sophisticated model resulted in convergence issues. Still, the wave digital model runtime was about 300 times faster on an identical computational device.

IV. Conclusion

In this work, we have considered the problem of a navigation processor trying to find the shortest path in a maze between entry and exit. The electrical interpretation exploits the inherent nature of the current to find the path of least resistance. We have extended existing results by presenting an electrical circuit design that utilizes models of real RRAM-cells to properly describe the shortest path problem. We have developed a wave digital emulation algorithm that could be implemented on a DSP or FPGA to operate in real time. Our simulation results have shown that the proposed setup solves the problem of the navigation processor efficiently in many different scenarios. This application example has revealed that the wave digital algorithm is an essential and powerful tool for the emulation of self-organizing circuits to reduce costs and development time before the manufacturing process.

Acknowledgment

The financial support by the German Research Foundation (Deutsche Forschungsgemeinschaft - DFG) through FOR 2093 and DFG-404291403 is gratefully acknowledged.

References

[1] K. Ochs *et al.*, "Anticipation of Digital Patterns," *International Journal of Circuit Theory and Applications*, vol. 46, pp. 235 – 243, Feb. 2018.

[2] Y. Pershin *et al.*, "Self-organization and Solution of Shortest-path Optimization Problems with Memristive Networks," *Physical review. E, Statistical, nonlinear, and soft matter physics*, vol. 88, no. 1, pp. 013 305 1 – 8, Jul. 2013.

[3] Y. Pershin, "Solving Mazes with Memristors: A Massively Parallel Approach," *Physical Review*, vol. 84, no. 4, p. 046703, Oct. 2011.

[4] G. Nui *et al.*, "Material Insights of HfO_2-based Integrated 1-Transistor-1-Resistor Resistive Random Access Memory Devices Processed by Batch Atomic Layer Deposition," *Scientific Reports 6*, p. 28155, Jun. 2016.

[5] L. Chua, "Everything You Wish to Know About Memristors But Are Afraid to Ask," *International Journal of Circuit Theory and Applications*, vol. 24, no. 2, pp. 319 – 368, Jun. 2015.

[6] V. Thangamani, "Memristor-Based Resistive Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design," *Control Theory and Informatics*, vol. 4, no. 7, pp. 7–14, 2014.

[7] R. Waser *et al.*, "Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges," *Advanced Materials*, vol. 21, no. 25-26, pp. 2632–2663, Jul. 2009.

[8] E. Bailey *et al.*, "Understanding Synaptic Mechanisms in $SrTiO_2$ RRAM Devices," *IEEE Transactions on Electron Devices*, pp. 1 – 7, 2018.

[9] S. Dirkmann *et al.*, "Understanding Filament Growth and Resistive Switching in Hafnium Oxide Memristive Devices," *ACS Applied Materials and Interfaces*, vol. 17, no. 10, pp. 14 857 – 14 868, Mar. 2018.

[10] R. Ranjan, "Programmable Memristor Emulator ASIC for Biologically Inspired Memristive Learning," *39th International Conference Telecommunications and Signal Processing*, pp. 261–264, Jun. 2016.

[11] C. Sànchez-López *et al.*, "A 860 kHz Grounded Memristor Emulator Circuit," *AEÜ International Journal of Electronics and Communications*, vol. 73, pp. 23–33, Mar. 2017.

[12] A. Fettweis, "Wave Digital Filters: Theory and Practice," *Proceedings of the IEEE*, vol. 74, no. 2, pp. 270–327, Feb. 1986.

[13] K. Ochs *et al.*, "Wave Digital Emulation of a Double Barrier Memristive device," *IEEE 59th International Midwest Symposium on Circuits and Systems*, pp. 1–4, Aug. 2016.

[14] K. Ochs *et al.*, "Wave Digital Emulation of Charge- or Flux-Controlled Memristors," *IEEE 59th International Midwest Symposium on Circuits and Systems*, pp. 1–4, Aug. 2016.

[15] E. Solan *et al.*, "Wave Digital Emulation of General Memristors," *International Journal of Circuit Theory and Applications*, pp. 1–17, Jul. 2018.

[16] E. Solan *et al.*, "Wave Digital Emulation of a $TiN/Ti/HfO_2/TiN$ RRAM Cell Based on a Semi-Physical Model," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, Feb. 2019.

[17] K. Ochs, "Passive Integration Methods: Fundamental Theory," *AEÜ International Journal of Electronics and Communications*, vol. 55, no. 3, pp. 153–163, May 2001.