Solving the Longest Path Problem using a HfO_2-based Wave Digital Memristor Model

Karlheinz Ochs, Dennis Michaelis, and Enver Solan

Ruhr-University Bochum
Chair of Digital Communication Systems
Bochum, Germany
Email: {karlheinz.ochs, dennis.michaelis, enver.solan}@rub.de

***Abstract*—Since electrical circuits are known to be inherently massively parallel architectures, circuit-inspired approaches are potential candidates to solve computationally complex problems. One of these problems is discovering all possible paths through a maze, which includes the shortest and the longest path, where finding the latter is known to be a np-complete problem. The key towards an efficient solution to the problem are self-organizing memristive circuits. Utilizing memristors – resistors with a memory – has shown to outperform all existing graph-theoretical algorithms and while theoretical models of memristors have been used to tackle the maze problem before, it has not been addressed by using models of real, manufacturable memristors. This paper intends to employ physical models of a real resistive random access memory (RRAM) memristive devices that are known for their fast switching behavior to find the longest path through a maze. We exploit the wave digital concept to create a real-time capable algorithm that has a direct correspondence to an electrical circuit. The emulation results show the counterintuitive result that the size of the maze has a negligible influence on the time the solution is found.**

I. Introduction

Self-organizing circuits are of particular interest in current research, as they enable machine-learning [1]. Computationally complex problems, such as np-hard an np-complete problems, are potentially efficiently solvable by circuit-inspired solutions due to their massively parallel architecture [2]. One of these problems is finding the longest path between the entry and exit node of a maze. The here exploited analog parallelism is different from computational parallelism and enables finding the solution to the problem in only a single step, outperforming all known graph-theoretical algorithms [2]. The essential devices to enable the desired functionalities in such circuits are memristors [3]. Circuit solutions to the maze problem have only been investigated with theoretical models of memristors. We aim to provide a solution that is based on physical models of real memristive devices. RRAM-cells are known for their rapid switching behavior which is beneficial in time critical problems such as computationally intensive applications. Although commonly used in the context of memory utilization [4], [5], RRAM-cells became popular in self-organizing circuits since their interpretation as memristive devices [6]. HfO_2-based RRAM-cells are subject to current research and their switching behavior is well investigated [7], making them a suitable choice for the examinations in this work.

Nevertheless, investigations on real memristive devices are expensive and they are often substituted by operational amplifier based emulators [8], [9]. During a development process it is beneficial to exploit more flexible real-time capable algorithm based emulators. Here, we prefer wave digital emulators because they have a direct correspondence to the underlying physics and they preserve energetic properties such as passivity [10], [11]. These emulators have successfully been used in a variety of different applications [12]–[15] and can be implemented on a digital signal processor (DSP) or a reconfigurable field programmable gate array (FPGA) to emulate for example RRAM-cells embedded in an analog circuit.

The paper is structured as follows. In Sec. II we discuss the circuit utilized to solve the longest path problem in a maze of arbitrary size and provide details on the deployed RRAM-cell. In Sec. III the wave digital model of this circuit is developed, before the emulation results in Sec. IV confirm the proper solutions to the problem. A final conclusion summarizes the main contributions.

II. Circuit Description of the Maze Problem

In this work we investigate a maze which generally is a collection of obstacles placed in between an entry and an exit with the goal to aggravate finding one or multiple paths from the former towards the latter. In the following, a structural circuit description of an arbitrary $n \times m$ maze is given. First, we define a grid of nodes for the maze, as can be seen in Fig. 1. Every two neighboring nodes are connected via a one-port connection element $\mathcal{N}_\kappa$ whose purpose is to create an open loop in case there is a wall or a finite resistance in case the path is passable. If one applies a voltage $u > 0$ between entry node φ_ν and exit node φ_μ, a current will flow along every possible path between φ_μ and φ_ν. This behavior motivates a RRAM-based connection element since their transition speed between the high and low resistance state is voltage dependent.

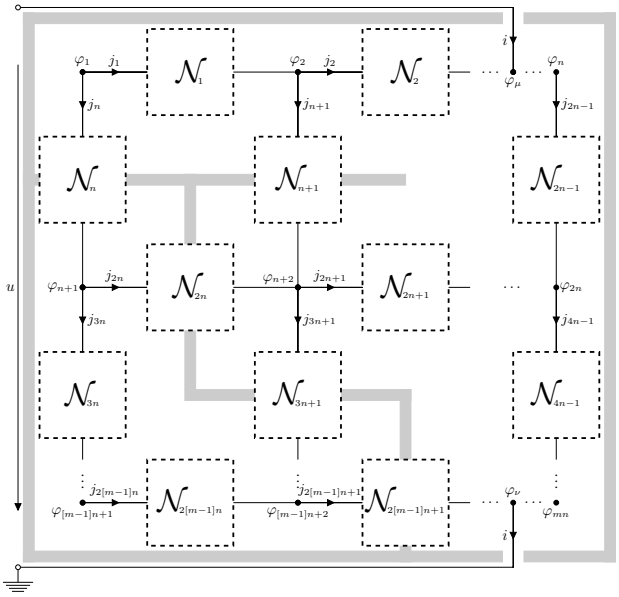

Fig. 1. Overall description of a $n \times m$ maze whose topology is indicated by the gray bars. Between every two neighboring nodes there is a connection element which indicates whether the transition from one neighboring node to another is valid (no wall) or invalid (wall). The input and output nodes are φ_μ and φ_ν, respectively. The input signal u will cause a current to flow through every path between φ_μ and φ_ν.

A. Memristive Connection Element

For the memristive connection element we utilize a voltage-controlled, HfO_2-based RRAM-cell, which is discussed in detail in [14] and is shown in Fig. 2 (left). The relationship between current and voltage is given by

$$j = W(z, v)\, v, \tag{1a}$$

$$W(z, u) = W_1 + z[W_0(v) - W_1], \tag{1b}$$

where $W(z, v)$ is the memductance and the high conductance state (HCS) W_1 and the low conductance state (LCS) $W_0(v)$ of the RRAM-cell are achieved when $z = 0$ and $z = 1$, respectively. The state equation for the inner state z is described by

$$\dot{z} = g(u)[\sigma(u)\sigma(z) + \sigma(-u)\sigma(1 - z)], \tag{1c}$$

$$g(u) = S_\mathrm{p}\Sigma(u - U_\mathrm{tp}) + S_\mathrm{n}\Sigma(u - U_\mathrm{tn}), \tag{1d}$$

where $\sigma(\xi)$ is the Heaviside function, $\Sigma(\xi) = \int_0^\xi \sigma(\eta)\mathrm{d}\eta$, S_n and S_p describe the steepness of transitioning from W_1 to $W_0(v)$ and vice versa, respectively, and U_tn and U_tp are the negative and positive thresholds for the transition behavior, respectively. It furthermore applies that

$$W_1 = NG_\mathrm{q}, \text{ and } G_\mathrm{q} = \frac{i_0}{u_0}, \tag{2}$$

where N is the number of conducting paths through the memristive layer and G_q, i_0, u_0 are normalization constants with the physical units of a conductance, current and voltage, respectively. The LCS is

$$W_0(u) = \frac{G_\mathrm{q}u + i_0 \ln\left(\frac{1+e^{\gamma-\beta u/u_0}}{1+e^{\gamma+[1-\beta]u/u_0}}\right)}{u}, \tag{3}$$

where γ describes the potential barrier between conducting filaments and β the voltage division ratio between pre and post potential barrier.

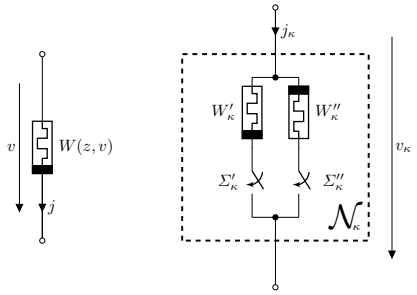

Fig. 2. Utilized model of the HfO_2-based RRAM-cell (left) and connection element $\mathcal{N}_\kappa$ (right), represented as a one-port with external current j_κ and voltage u_κ.

The connection element $\mathcal{N}_\kappa$ utilizing the physical model of the RRAM-cell described above is shown in Fig. 2 (right). The anti-parallel interconnection of two RRAM-cells W'_κ and W''_κ together with the two switches Σ'_κ and Σ''_κ enables the following different operation modes. If both Σ'_κ and Σ''_κ are closed, the connection element represent a bidirectional path, while having both Σ'_κ and Σ''_κ in the open state represents a wall since no current can flow. If either Σ'_κ is closed and Σ''_κ is open, or vice versa, it represents a one-way street within the labyrinth.

B. Maze Description

We define node potentials $\boldsymbol{\varphi}$ and branch currents $\boldsymbol{j}$

$$\boldsymbol{\varphi} = [\varphi_1, \ldots, \varphi_{mn}]^T, \quad \boldsymbol{j} = [j_1, \ldots, j_{2mn-1}]^T. \tag{4}$$

If node φ_μ and node φ_ν are the entry and exit of the maze, as shown in Fig. 1, then the voltage u is the potential difference between node $\varphi_\mu = u$ and grounded node $\varphi_\nu = 0$. The branch voltages $\boldsymbol{v}$ are obtained by the respective node potential differences and can be expressed as

$$\boldsymbol{v} = \boldsymbol{N}^T\boldsymbol{\varphi}(u), \tag{5}$$

where $\boldsymbol{N}$ is the incidence matrix of the circuit in Fig. 1. Consequently, by Tellegen's theorem, the relationship between branch currents $\boldsymbol{j}$ and the node currents $\boldsymbol{i}$ is

$$\boldsymbol{i} = \boldsymbol{N}\boldsymbol{j}, \tag{6}$$

where $i = -\boldsymbol{e}_\mu^T\boldsymbol{i} = \boldsymbol{e}_\nu^T\boldsymbol{i}$. The connection element relation is expressed with the help of (5), as

$$\boldsymbol{j} = \boldsymbol{W}(\boldsymbol{z}, \boldsymbol{v})\, \boldsymbol{v}, \tag{7}$$

where $\boldsymbol{W}(\boldsymbol{z}, \boldsymbol{v}) = \mathbf{diag}(W_\kappa(z_\kappa, v_\kappa))$, $\kappa = 1, \ldots, 2mn - 1$, with W_κ being the total admittance value of the κ-th connection element as depicted in Fig. 2 (right). With (5) and (6), we get

$$\boldsymbol{i} = \boldsymbol{N}\boldsymbol{W}(\boldsymbol{z}, \boldsymbol{N}^T\boldsymbol{\varphi}(u))\, \boldsymbol{N}^T\boldsymbol{\varphi}(u), \tag{8}$$

which is a nonlinear set of equations that could also be obtained via via mesh current or node potential method and is numerically solvable.

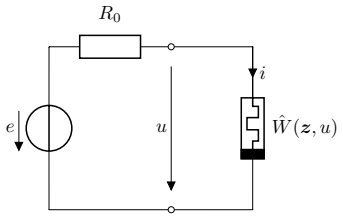

Fig. 3. One-port representation of the maze in Fig. 1 with resistive voltage source.

Consequently, the memristive network between nodes φ_μ and φ_ν can be described by a single one port memristor $\hat{W}(\boldsymbol{z}, u)$ shown in Fig. 3 as indicated by the closure theorem in [3]. This depiction is particularly beneficial for a compact wave digital signal flow graph, which we derive in the following section.

III. Wave Digital Representation

The wave digital concept is here exploited as an emulation technique as it is known to preserve energetic properties such as passivity in a digital signal processing sense [10]. It leads to an computationally massive parallel algorithm which can be implemented on DSPs and FPGAs for real-time applications in integrated circuits.

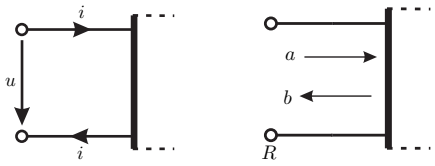

Fig. 4. Definition of a port with electrical quantities u, i (left) and wave quantities a, b with port resistance R (right).

Voltage u and current i of Fig. 4 are related to incident wave a and reflected wave b via an arbitrary constant $R > 0$ that is called the port resistance and the bijective transformation

$$\begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} 1 & R \\ 1 & -R \end{bmatrix} \begin{bmatrix} u \\ i \end{bmatrix}. \tag{9}$$

The resistive voltage source in Fig. 3 is expressed in wave quantities by

$$u = e - R_0 i \quad \Leftrightarrow \quad a = e, \tag{10}$$

if the port resistance is chosen such that $R = R_0$. The memristor in Fig. 3 can be expressed as

$$i = \hat{W}(\boldsymbol{z}, u)u \quad \Leftrightarrow \quad b = \rho(\boldsymbol{z}, u)a, \tag{11}$$

where the reflection coefficient is

$$\rho(\boldsymbol{z}, u) = \frac{1 - R_0\hat{W}(\boldsymbol{z}, u)}{1 + R_0\hat{W}(\boldsymbol{z}, u)}. \tag{12}$$

The overall wave digital signal flow graph is depicted in Fig. 5 and contains a parametric loop that is highlighted in orange. We address these numerically by fix-point iterations [14].

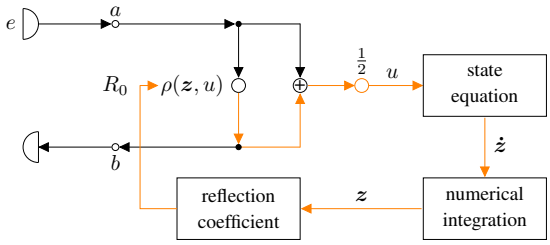

Fig. 5. Wave digital flow graph of the setup in Fig. 3 with the parametric loop highlighted in orange.

IV. Emulation Results

In the following we compare two mazes of different size in regard to the finding of their optimal paths to verify the proper solution to the longest path problem with the utilization of a physical model of a RRAM-cell. The emulation results are shown in Fig. 6, the emulation parameters are in Table I.

Emulation parameters					
i_0	=	38.74 μA	R_0	=	10 kΩ
u_0	=	0.5 V	S_p	=	-50 Hz/V
N	=	1.5	S_n	=	-0.4 Hz/V
β	=	0.1	U_tp	=	1 V
γ	=	3.8	U_tn	=	-0.5 V

TABLE I
Parameters for the emulation results in Fig. 6.

The setup for scenario 1 is displayed in the left of Fig. 6. It is a 20×20 maze which consequently contains 361 connection elements and therefore 722 RRAM-cells. After applying an input signal of $e \equiv 180\,\mathrm{V}$, three possible paths of different lengths between the entry and exit node of the maze are found which are highlighted in green, orange and blue, respectively. Since the shortest path (orange) contains the least amount of connection elements, its memristors experience the highest voltage and hence switch to the HCS faster than the memristors of any other path. For this reason we observe a discontinuity in the course of the current at $t \approx 13\,\mathrm{ms}$ which is displayed at the top right of Fig. 6. This is the exact time when all according memristors of the orange path have transitioned to the HCS.

Consequently, when we observe the other two discontinuities at $t \approx 32\,\mathrm{ms}$ and $t \approx 39\,\mathrm{ms}$, we know that this is when all according memristors of the middle path (green) and those of the longest path (blue) have transitioned in the HCS, respectively. Therefore, all possible paths between entry and exit node are found in ascending order, from the shortest path to the longest path, which solves the np-complete problem of finding the longest path (and simultaneously all other paths). In general, in a maze where the path length of all possible path differs greatly, those paths will likely be found in ascending order. But even in mazes where the order is not related to the path length, one will find all possible paths and can reverse engineer which is the longest amongst them. Because the longest path can at most have length $n \cdot m$, one can simply

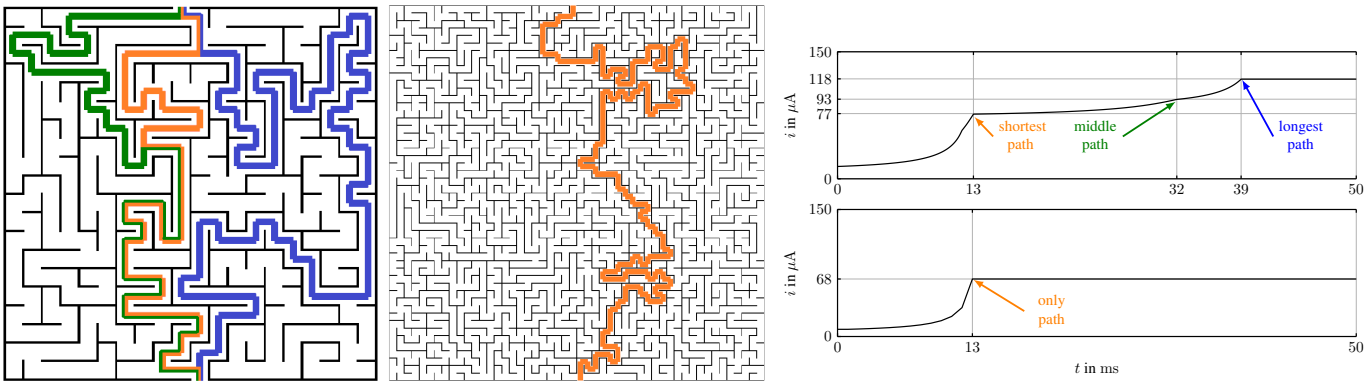

Fig. 6. Comparison of a 20×20 maze with three possible paths from entry to exit, highlighted in orange, green and blue (left) and a 50×50 maze with only a single path (middle). The course of the currents for the 20×20 and 50×50 maze are shown at the top right and bottom right, respectively.

choose the input signal e to be large enough such that even a path of this length would be found.

Scenario 2 involves a 50×50 maze which contains 2401 connection elements and in consequence 4802 RRAM-cells, which are over 6 times as many as the setup of scenario 1. After applying an input signal of $e \equiv 500\,\mathrm{V}$, it can be noted that this maze only contains a single path between entry and exit node. Although it contains many more RRAM-cells and even the path length is significantly longer than in the first scenario, the time at which the path is found is also $t \approx 13$ ms which is the exact time the shortest paths was found in the smaller maze. This leads to the counterintuitive conclusion that the size of the maze has a negligible influence on the convergence time. This is due to the inherently massive analog parallelism and is the reason why computationally complex problems as the one investigated in this work can be solved efficiently by memristive circuits.

V. Conclusion

In this work, we have considered the np-complete problem of finding the longest path in a maze of arbitrary size. Because memristive circuits are known to solve computationally complex problems efficiently, we have interpreted the investigated problem in an electrical circuit containing physical models of RRAM-cells, which are a popular choice for run-time critical applications due to their rapid switching behavior. The wave digital concept has been exploited as an emulation technique to obtain a real-time capable algorithm that could be implemented on a DSP or FPGA for future research. Our emulation results have shown that the longest path in the maze is found reliably and all other possible paths are found simultaneously. Furthermore, it was observed that the size of the maze has no influence on the convergence time of the circuit.

For future work, it is desirable to manufacture a memristor with a lower threshold voltage to decrease the required amplitude of the input signal. Additionally, the here established software emulator allows for a sensitivity analysis with parameter variances in the memristive elements to obtain further insights.

Acknowledgment

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