Circuit Synthesis and Electrical Interpretation of Synchronization in the Kuramoto Model

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***Index Terms*—Synchronization, circuit synthesis, wave digital model, emulation, circuit theory.**

***Abstract*—Kuramoto oscillator systems are well-studied models to investigate the synchronization process of coupled oscillators in a wide variety of contexts, among them neural networks. The current trend of neuromorphic systems demands electrical circuits for reasons of efficiency, low costs, and high speed. The goal of this work is to study the Kuramoto model with arbitrary coupling structure from a circuit theoretical perspective. For this reason, we synthesize an ideal electrical circuit based on the Kuramoto model which enables an electrical interpretation of its synchronization behavior. Because of the knowledge of voltage, current and power flows in (ideal) electrical devices, circuit synthesis in general can offer perspectives and interpretation that might not be attainable from system theory. We therefore see the structured approach of the synthesis and its electrical interpretation of the well-known Kuramoto model as a general procedure that will increase insights and diversify understanding on neural networks. To achieve this, we utilize the wave digital concept here which offers an especially intuitive view on power flow.**

I. Introduction

The synchronization of physical, biological, chemical or social systems has always been an interesting topic for in-depths research. The arguable largest recent interest in this regard has been in the context of neuronal networks where the learning behavior is associated with the synchronization process of neuron groups [1].

An often deployed and well-studied model to investigate general synchronization processes between fully connected populations of oscillators is the Kuramoto model [2]. It is especially popular in the field of automatic control and despite its existence for decades it is subject of current research [3]–[5]. Because synchronization processes in general are essential to study learning behavior in the context of machine learning [6], [7] and to better understand human learning [8]. Large-scale neural networks require an electrical circuit-based implementation due to their complexity. Electrical circuits require less space, run more energy-efficient than software solutions, can operate faster and scale better with increasing complexity due to their analog massively parallelism [9]. With a vast runtime advantage and the massive parallelism, circuit-based solutions are candidates to solve problems that could not be solved by systems which execute tasks successively [10].

The wave digital concept [11] is often exploited to obtain massively parallel, real time capable algorithms of electrical circuits that can be run on digital signal processors or field programmable gate arrays and are integrable in embedded systems. The concept is also often exploited to create emulators, aiding development and manufacturing processes besides increasing understanding of circuits. It can even be used as a modeling tool [12].

For these reasons we synthesize an ideal electrical circuit of the well-established Kuramoto model with the goal to derive a wave digital model on the one hand and gain deeper insights of the synchronization processes on the other hand. While basic synchronization patterns of the Kuramoto model are system theoretically well-investigated and circuit implementations with operational amplifiers exist [13], we extend existing results with the electrical interpretation and understand the here presented circuit theoretical procedure as an universal tool that can be applied in other contexts where synchronization behavior is of interest.

In Sec. II an electrical circuit is systematically synthesized from the state-space model of the Kuramoto oscillator system and is utilized to obtain an electrical interpretation of the synchronization condition. The wave digital representation is discussed in Sec. III, before the simulation results in Sec. IV verify our findings of the electrical circuit and interpretation of synchronization. The final conclusion in Sec. V summarizes the main results.

II. Circuit Synthesis of the Kuramoto Model

A. The Kuramoto Model

A system of n coupled Kuramoto oscillators are described by the state-space model

$$\Sigma_{\text{Kuramoto}}: \begin{cases} \dot{\varphi}_\mu &= \omega + \frac{\Omega_\text{c}}{n} \sum_{\nu=1}^{n} \sin(\varphi_\nu - \varphi_\mu), \\ z_\mu &= \varphi_\mu, \\ y_\mu &= \sin(\varphi_\mu), \end{cases} \tag{1}$$

where $\mu = 1, \ldots, n$, φ_μ is the angle of the μ-th oscillator, ω is the intrinsic natural frequency in rad, Ω_c is the coupling factor in s^{-1}, z_μ is one output required to convey the information about the μ-th state to the neighboring oscillators, and y_μ is the

output of interest for observation. Note that the state equation itself is not describing an oscillator, but an integrator. The reason we observe oscillation is because of the trigonometric relationship between the state φ_μ and the output y_μ.

B. Electrical Synthesis

The state equation of the overall system (1) can be divided into the proper motion ω and the input signal $\frac{\Omega_\mathrm{c}}{n}\sum_{\nu=1}^{n}\sin(\varphi_\nu-\varphi_\mu)$. By associating φ_μ with the voltage u_μ we will show that the circuits in Fig. 1 describe the proper motion and the input signal of (1), respectively.

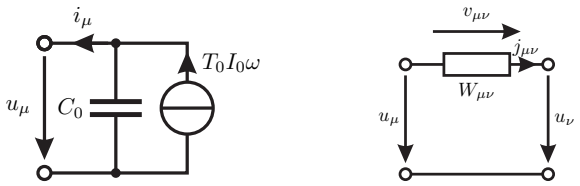

Fig. 1. Integrator circuit with the underlying differential equation (2) (left) and a resistive coupling element to describe one summand of (3), i.e. the input signal of integrator μ from integrator ν (right).

The underlying differential equation of the integrator circuit in Fig. 1 (left) is

$$\dot{u}_\mu = [T_0 I_0 \omega - i_\mu]/C_0, \tag{2}$$

where $C_0,\ T_0,\ I_0$ are normalization constants with the physical units of a capacitance, time and a current, respectively. In order to fulfill the state equation of (1) it is then required that

$$i_\mu = -I_0\frac{\Omega_\mathrm{c}}{N}\sum_{\nu=1}^{N}\sin\left(\frac{u_\nu-u_\mu}{U_0}\right), \tag{3}$$

with U_0 being a normalization constant with the physical unit of a voltage. From Fig. 1 (right) one obtains that

$$j_{\mu\nu} = W_{\mu\nu}v_{\mu\nu} = W_{\mu\nu}[u_\mu - u_\nu], \tag{4}$$

with $\mu<\nu$.

Let $j_{\mu\nu}$ be the input signal at integrator μ from integrator ν, such that Kirchhoff's current law yields to

$$\boldsymbol{i} = \boldsymbol{N}\boldsymbol{j}, \quad \Leftrightarrow \quad \boldsymbol{v} = \boldsymbol{N}^T\boldsymbol{u}, \tag{5}$$

where $\boldsymbol{i}$ is the vector of all currents $i_\mu,\ \mu=1,\dots,n$, $\boldsymbol{j}$ the vector of all currents $j_{\mu\nu},\ \mu,\nu=1,\dots,n,\ \mu<\nu$, and $\boldsymbol{N}$ is the incidence matrix. The equivalence is obtained through Tellegen's theorem, where $\boldsymbol{u}$ is the vector of all voltages u_μ and $\boldsymbol{v}$ the vector of all currents $v_{\mu\nu}$.

In order to determine the admittances $W_{\mu\nu}$ we observe through (5) that the current i_μ is the sum of all $j_{\mu\nu}$ which are incident to oscillator μ and therefore conclude that $j_{\mu\nu}$ accounts for the exchange between integrators μ and ν. Consequently, it is desired that $j_{\mu\nu} = -I_0\frac{\Omega_\mathrm{k}}{n}\sin\left(\frac{u_\nu-u_\mu}{U_0}\right)$ and by (4) it holds that

$$W_{\mu\nu} = G_0 T_0 \frac{\Omega_\mathrm{c}}{n}\mathrm{si}\left(\frac{u_\nu-u_\mu}{U_0}\right), \tag{6}$$

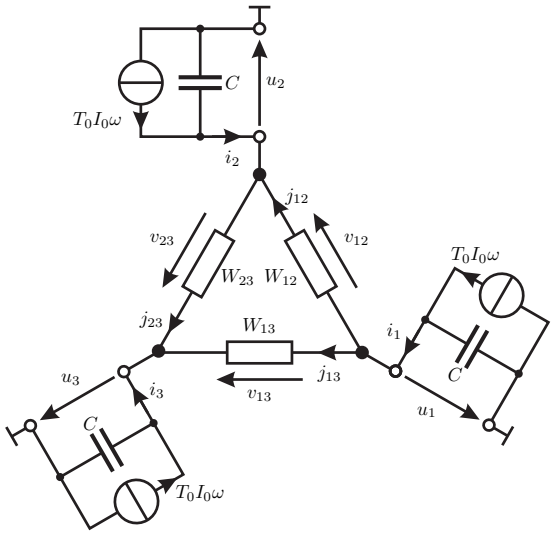

Fig. 2. Complete setup of a system consisting of $n=3$ Kuramoto oscillators.

with G_0 having the physical unit of an admittance. A Kuramoto model of three fully coupled integrators is shown in Fig. 2. A condensed formulation of (4) is

$$\boldsymbol{j} = \boldsymbol{W}_0\boldsymbol{v}, \tag{7}$$

with $\boldsymbol{W}_0 = \mathrm{diag}(W_{\mu\nu}),\ \mu,\nu=1,\dots,n,\ \mu<\nu$.

We then can translate the interconnection network's internal variables, currents $\boldsymbol{j}$ and voltages $\boldsymbol{v}$, to the external currents $\boldsymbol{i}$ and voltages $\boldsymbol{u}$ with the incidence matrix $\boldsymbol{N}$, resulting in

$$\boldsymbol{i} = \boldsymbol{W}\boldsymbol{u},\ \text{with}\ \boldsymbol{W} = \boldsymbol{N}\boldsymbol{W}_0\boldsymbol{N}^T. \tag{8}$$

Note that through (8), since $\boldsymbol{W}$ contains topology information through $\boldsymbol{N}$, it is not only possible to investigate a fully connected topology but allows for any topology such as self-coupling, chain or ring topologies.

III. Wave Digital Representation

In the following we derive the wave digital model of the electrical circuit that is shown exemplarily in Fig. 2 with $n=3$ oscillators. We omit some details for the sake of brevity and refer the interest reader to [11].

To obtain a wave digital model, the electrical circuit is decomposed port-wise and then translated port-wise into the wave digital domain. The relation between voltage, current and wave quantities at such a port is described by

$$\begin{aligned} a &= u + Ri, \quad u = [a+b]/2, \\ b &= u - Ri, \quad i = [a-b]/[2R], \end{aligned} \tag{9}$$

where a is the incident wave, b the reflected wave, and $R>0$ an arbitrarily chosen positive constant called port resistance, see Fig. 3.

A. Integrator Circuit

Fig. 4 shows the integrator circuit of Fig. (1) (left) and its wave digital representation, where R, R_Q, R_C are the respective port resistances.

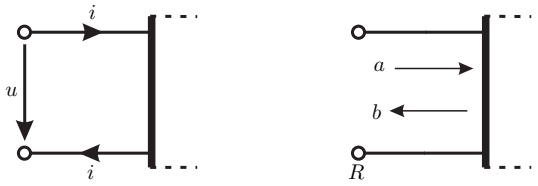

Fig. 3. Definition of a port with current i, voltage u, incident wave a, reflected wave b and port resistance R.

The ideal current source can be represented through

$$i_\mu = T_0 I_0 \omega \quad \overset{(9)}{\Leftrightarrow} \quad b_{Q\mu} = a_{Q\mu} - 2T_0 I_0 R_Q \omega.$$

From (9) and passive integration through the trapezoidal rule, a capacitor translates to a delay element in the wave domain. The parallel interconnection of capacitor and ideal current source is enabled by a parallel adaptor, with

$$\begin{bmatrix} a_{C\mu} \\ a_{S\mu} \\ a_{Q\mu} \end{bmatrix} = \begin{bmatrix} \gamma - 1 & 1-\gamma & 1 \\ \gamma & -\gamma & 1 \\ \gamma & 1-\gamma & 0 \end{bmatrix} \begin{bmatrix} b_{C\mu} \\ b_{S\mu} \\ b_{Q\mu} \end{bmatrix}, \text{ and } \gamma = \frac{R}{R + R_C}.$$

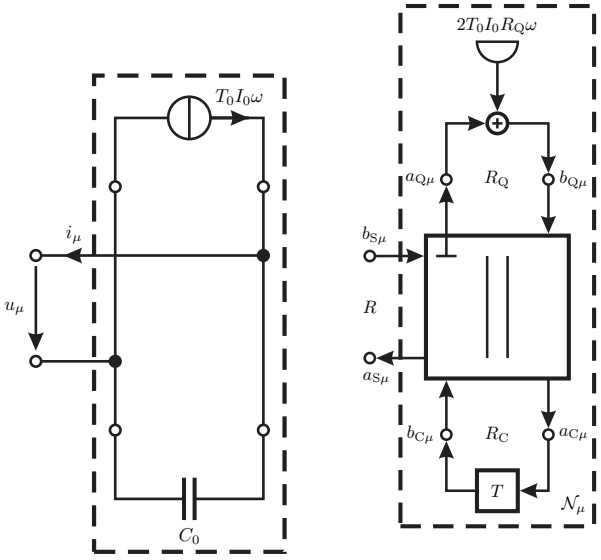

Fig. 4. Integrator circuit described by (2) (left) and its wave digital representation (right).

B. Interconnection network

With (8), one obtains the wave representation by

$$\boldsymbol{i} = \boldsymbol{W}\boldsymbol{u} \quad \overset{(9)}{\Leftrightarrow} \quad \boldsymbol{b} = [\boldsymbol{G}_0 + \boldsymbol{W}]^{-1}[\boldsymbol{G}_0 - \boldsymbol{W}]\boldsymbol{a} = \boldsymbol{S}\boldsymbol{a}, \quad (10)$$

where $\boldsymbol{G}_0 = R^{-1}\mathbf{1}$. $\boldsymbol{S}$ can be factorized through Householder or Givens transformation to obtain a reference circuit consisting of two-port parallel adaptors and transformers [14].
This enables a convenient general description of the overall setup shown in Fig. 5, where $\boldsymbol{a}_S = [a_{S1}, \ldots, a_{SN}]^T$ and $\boldsymbol{b}_S = [b_{S1}, \ldots, b_{SN}]^T$.

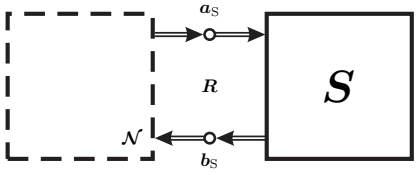

Fig. 5. General description of n Kuramoto oscillators $\boldsymbol{\mathcal{N}}$ interconnected via a general topology described by the scattering matrix $\boldsymbol{S}$.

IV. Electrical Interpretation of Synchronization Condition

From [2] it is known that synchronization is achieved if

$$\sum_{\nu=1}^{N} \sin(\varphi_\nu - \varphi_\mu) \overset{!}{=} 0, \text{ mit } \mu = 1, 2, ..., n. \quad (11)$$

As the left hand term of (11) is directly correlated to the currents i_μ, see (3), it follows that

$$\boldsymbol{i} = \boldsymbol{0}. \quad (12)$$

Note that this is only a sufficient condition, as there three scenarios which satisfy (11) and consequently (12), only one of which is the normally desired complete synchronization. The other two scenarios which bring the synchronization process to a halt are here referred to as *anti-phase* and *zero sum*.

1) Anti-phase Configuration: A pure anti-phase configuration requires a precise phase shift between every possible pair of oscillators of

$$u_\mu - u_\nu = \pm U_0 \pi, \ \mu, \nu = 1, \ldots, n, \ \mu \neq \nu, \quad (13)$$

which is only possible to achieve for exactly $n = 2$ oscillators. Plugging (13) into (6) yields to

$$W_{\mu\nu} = G_0 \frac{\Omega_c}{n} \mathrm{si}(\pm\pi) = 0.$$

Therefore, is follows that $\boldsymbol{W} = \boldsymbol{0}$ and consequently, by (8), that (12) is satisfied. Viewed from an electrical perspective, $\boldsymbol{W} = \boldsymbol{0}$ translates to an open-loop between the oscillators. As a consequence, no current can flow. Fig. 6 shows the simulations results for two oscillators in the anti-phase configuration. The initial conditions are such that $\varphi_1(0) = -\varphi_2(0)$ which corresponds to a phase shift of π. We like to point the

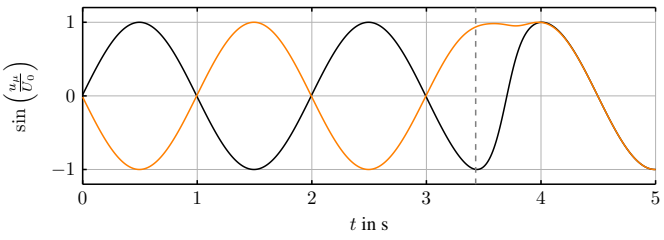

Fig. 6. Two oscillators in the anti-phase configuration. Since their phase shift is exactly π, the admittance in Fig. 1 (right) is 0.

reader to $t \approx 3.5$ s, where the setup converges to complete

synchronization. This is due to the finite precision of the computational entity used to obtain the simulation results, as a perfect anti-phase configuration would require infinite precision.

2) Zero Sum Configuration: In this scenario the currents in the interconnection network are circulating internally yet they vanish externally

$$j_{\mu\nu} \neq 0, \text{ but } \boldsymbol{i} = \boldsymbol{N}\boldsymbol{j} = \boldsymbol{0},$$

because currents $j_{\mu\nu}$ are such that $\boldsymbol{j}$ is orthogonal to the incidence matrix $\boldsymbol{N}$. These conditions imply that a subset of the conductances in the interconnection network must become negative (i.e. the interconnection network becomes internally active, but remains externally passive). For example, in Fig. 2, if

$$u_\mu = u_1 + U_0[k-1]\frac{2\pi}{n}, \quad k = 1, \ldots, n,$$

it results in $j_{12} = j_{23} = -j_{13}$. In order for $j_{13} < 0$, it is required that $W_{13} < 0$. In fact, the condition for a conductance $W_{\mu\nu}$ to be active is

$$\Delta v_{\mu\nu} = u_\mu - u_\nu > \pi \Leftrightarrow W_{\mu\nu} < 0,$$

since the si-function is negative under this implication.

The three oscillator setup of Fig. 2 in a zero sum configuration is displayed in Fig. 7 (top). The initial conditions are chosen such that they satisfy $\varphi_\mu(0) - \varphi_\nu(0) = \frac{2\pi}{3}$, $\mu, = 2, 3$, $\nu = \mu - 1$, which are the only possible sets of initial conditions for a three oscillator setup to be in a zero sum configuration. Fig. 7 (bottom) confirms these results: Since $j_{12} = j_{23} = -j_{13}$ we observe that the current internally circulates in the interconnection network with $W_{13} < 0$, indicating that it is internally active. However, due to (7), one can conclude that the interconnection network remains passive externally.

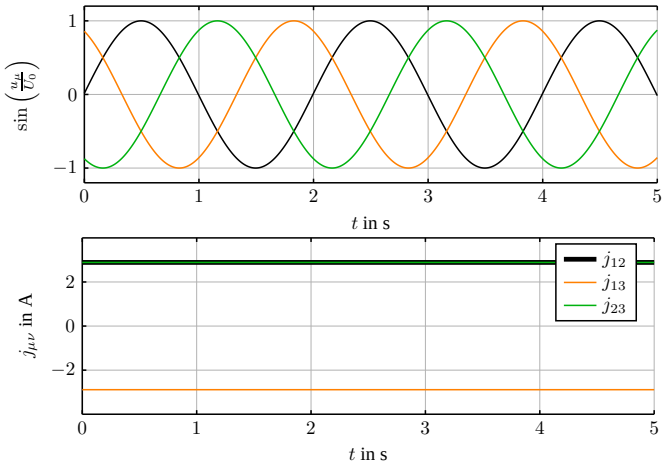

Fig. 7. The three oscillators of Fig. 5 in a zero sum configuration (top). As stated above, the interconnection network in this scenario is internally active while remaining externally passive, as can be seen from not all currents $j_{\mu\nu}$ being positive (bottom).

3) Complete Synchronization Configuration: Complete synchronization is synonymous with all states being identical, hence

$$\boldsymbol{u} = \boldsymbol{1}U \quad \Leftrightarrow \quad \boldsymbol{N}^T\boldsymbol{u} = \boldsymbol{0},$$

since the column sum of the incidence matrix is 0 by definition and hence voltages u_μ are such that $\boldsymbol{u}$ is orthogonal to $\boldsymbol{N}^T$. Therefore, by (8), it follows that (12) is satisfied.

Fig. 8 shows a two oscillator setup in an anti-phase configuration with a third oscillator acting as a relay to aid the synchronization process. Note that without the third oscillator the two oscillator would not synchronize completely as it has been established in Fig. 6. It must hold that $\varphi_3(0) \neq \varphi_\mu(0)$, $\mu = 1, 2$, since otherwise only a mixture of anti-phase and complete synchronization would be achieved.

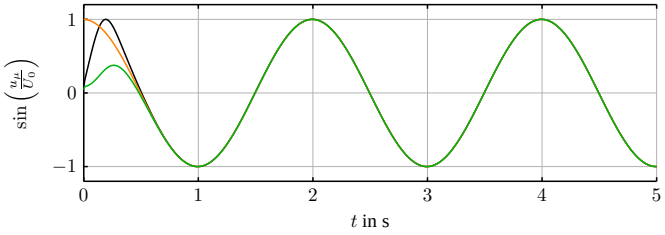

Fig. 8. Two oscillators in an anti-phase configuration with a third oscillator ensuring the transitioning to complete synchronization. This oscillator can be seen as a complete synchronization enabling relais oscillator.

V. Conclusion and Outlook

In this work, we have considered a system of Kuramoto oscillators for which an electrical circuit was synthesized. This step is crucial to obtain an electrical interpretation of the synchronization behavior of the coupled set of oscillators. We then derived a wave digital model of an arbitrarily coupled Kuramoto setup. Additionally, a runtime benefit can be obtained through the wave digital representation which will especially show in large-scale systems. Our simulation results confirm the proper derivation of the electrical circuit and its interpretation with respect to the synchronization behavior.

For future research, memristive coupling between the integrators, ideally with real memristive devices as in [15], is planned.

Acknowledgment

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