HfO$_2$-based Memristive Navigation Processor

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Chair of Digital Communication Systems
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Motivation

Optimization Problem

- solving a maze

State of the Art

sequentially operating algorithms

Von-Neumann bottleneck
effort increases with maze size

Possible Solution

exploiting analog parallelism of electrical circuits

How to realize a maze solving circuit?
Motivation

Optimization Problem
- solving a maze

Applications
- urban planning
- robotics
- machine learning
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E. Solan
26. March 2019
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Memristor

Resistive Random Access Memory - RRAM

Physical device

$\begin{align*}
\text{TiN} & \quad \text{Ti} \\
\text{HfO}_2 & \quad d_b \\
\text{TiN} & \quad \text{TiN}
\end{align*}$

- Hysteresis
- $10^{-4}$ to $10^{-1}$

Measurements

Average

LTspice Simulation

Parameter spread aggravates reproducible analysis.

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Memristor

Resistive Random Access Memory - RRAM

Physical device

- parameter spread aggravates reproducible analysis
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- simulation model is based on quantum-point-contact (QPC) theory
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- emulator for real-time capable applications
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Wave digital emulation
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Circuit Derivation

maze
Electrical Representation

Circuit Derivation

- maze
- regular grid
Circuit Derivation

- maze
- regular grid
- defining nodes
Electrical Representation

Circuit Derivation

- maze
- regular grid
- defining nodes
- connection elements
Connection Element

Circuit Derivation

Anti-parallel connection

- bidirectional behavior
- switches can be realized by transistors
  - maze topology creation
  - decoupling during read out operations
Circuit Derivation

Closure theorem of memristive networks facilitates wave digital emulation.
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Emulation Results

Shortest Path Solution

- massive parallel analog processing
- interwoven processor and memory
Emulation Results

Shortest Path Solution

- massive parallel analog processing
- interwoven processor and memory

Self-Organization

- self-organization because of memristors
- adaption to added/removed obstacles
Emulation Results

Shortest Path Solution

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Super-Efficiency

- effort is independent of maze size
- determined by switching time of one device
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Conclusion and Outlook

Conclusion

Hardware implementation

- RRAM-cell used as memristors
- no separation between storage and processing unit
- super-efficient solution based on massive analog parallelism

Wave digital emulator

- intermediate stage towards hardware realization
- robust and flexible algorithmic model
- sensitivity analysis and optimization

Outlook

- applications in related graph theoretical optimization problems
  - swarm intelligence
  - ant colony optimization
  - ...

Lehrstuhl für Digitale Kommunikationssysteme

E. Solan

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26. March 2019
Acknowledgment

Research Unit FOR 2093

The financial support by the German Research Foundation (Deutsche Forschungsgemeinschaft - DFG) through FOR 2093 is gratefully acknowledged.