

# Wave Digital Emulation of a Memristive Circuit to Find the Minimum Spanning Tree

Karlheinz Ochs, Dennis Michaelis, and Enver Solan

Ruhr-University Bochum  
Chair of Digital Communication Systems  
Bochum, Germany

Email: {karlheinz.ochs, dennis.michaelis, enver.solan}@rub.de

**Abstract**—Self-organizing circuits are subject to current research because they are known to solve computationally complex tasks fast, energy efficient and can be implemented in integrated circuits with minimum space requirements. This is especially desired in contexts where the problem involves many components, such as neural networks, and the solution demands exhaustive computational effort. Networks which are centered around memristors have shown to be good candidates for such self-organizing, circuit-inspired solutions. One of many interesting problems include finding the minimum spanning tree in a graph, as it has applications in human learning in the context of the self-organizing discovery of information transport and hence topology formation. This work presents a memristive circuit to solve the minimum spanning tree in a directed, weighted graph of arbitrary size. Since the manufacturing process of memristors is generally complicated and costly, a software emulator based on wave digital principles is derived which provides a powerful tool for investigations with different memristor models to aid development processes.

## I. INTRODUCTION

Self-organizing circuits generally are good candidates for solving computationally complex tasks and memristors – resistors with a memory – are the key elements in these circuits [1]. Such circuit-inspired, memristive solutions have shown to outperform graph-theoretical algorithms in different applications, such as finding all possible paths between the entry and exit node of a maze, where the problem can be solved in only a single step [2], [3].

Efficient solutions to graph-theoretical problems are of particular interest for current research on neural networks, as their deployed neuron models can be interpreted as vertices of a graph and the synapse models can be viewed as edges. Application examples of such neural networks include gait pattern generators [4], anticipation of digital patterns [5] or topology formation [6]. One amongst many graph-theoretical problems subject to investigation has been finding the shortest path between a starting vertex and all other vertices. Previous, non-circuit approaches to solve this problem exist, such as the Dijkstra, A\*, Bellman-Ford or Floyd-Warshall algorithms [7]. Among other features, these algorithms differ in their access to information on the topology and costs in the graph. A self-organizing solution to the minimum spanning tree problem is desirable in the context of unsupervised learning, as the

circuit itself discovers optimal communications structures for information transport. Unsupervised learning is also of interest in pattern recognition and circuit-based solutions have been found [8].

Emulators are currently used to develop and investigate memristive circuits, because the manufacturing process is costly and complicated. Wave digital emulators have shown to be beneficial for software emulations [9]–[11], especially because the wave digital method preserves passivity even under finite arithmetic conditions [12].

This work is structured as follows. In Sec. II the utilized memristor model is discussed and the memristive circuit solution to a fundamental graph is investigated in detail to highlight the basic functionality of the here presented approach. The wave digital emulator is derived in Sec. III and the emulation results of an example graph verify the proper function of the memristive circuits. A summary of our main results concludes the paper.

## II. MEMRISTIVE CIRCUIT SOLUTION TO MINIMAL SPANNING TREE PROBLEM

The goal of this work is to obtain a self-organizing, circuit-inspired solution to the minimum spanning tree problem, where a weighted, possibly directed graph  $\mathcal{G} = (\mathcal{V}, \mathcal{E})$  with a set of vertices  $\mathcal{V}$  and edges  $\mathcal{E}$  is given and the paths of lowest costs between a starting vertex and all other vertices is desired. Before we present our proposed memristive network to tackle this problem, we provide necessary details on the memristive elements which we deploy in this context.

### A. Vertex and Edge Memristive Elements

The relationship between current and voltage of the memristor in Fig. 1 is described by

$$i = W(z, u) u, \quad (1a)$$

$$W(z, u) = W_{\text{HCS}} + z[W_{\text{LCS}} - M_{\text{HCS}}], \quad (1b)$$

where  $W(z, v)$  is the memductance and  $z \in [0, 1]$  is the inner state, with  $z = 0$  indicating that the memristor is in the high conductance state (HCS)  $W_{\text{HCS}}$  and  $z = 1$  indicating that the

memristor is in the low conductance state (LCS)  $W_{LCS}$ . The state equation reads

$$\dot{z} = S[\sigma(u)\sigma(z) + \sigma(-u)\sigma(1-z)], \quad (1c)$$

where  $\sigma(\xi)$  is the Heaviside function and  $S$  is the steepness of the transition between  $W_{HCS}$  and  $W_{LCS}$  and vice versa.

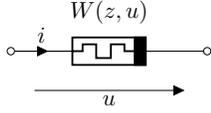


Fig. 1. Memristor with voltage  $u$ , current  $i$  and inner state  $z$ .

With the details explained in the following subsection, it is required for the application discussed here that the LCS and HCS of memristors deployed to represent the edge of between two vertices are different from the LCS and HCS of memristors used as a vertex representation. In fact, we will later show that

$$W_{HCS}^E \gg W_{HCS}^V \gg W_{LCS}^E \gg W_{LCS}^V, \quad (2)$$

must be satisfied. Therefore, both types of memristors utilized in this work are described by (1a)–(1c), and they only distinguish themselves by (2).

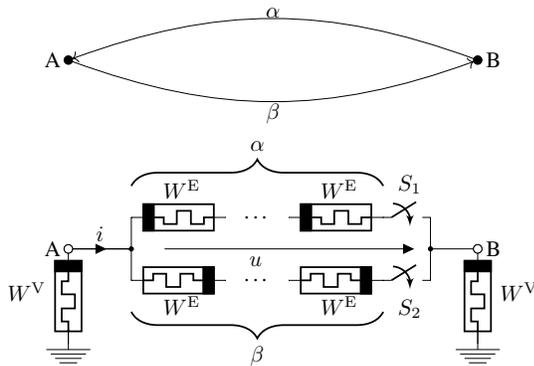


Fig. 2. Relationship between a graph representation with vertices  $A, B$  and edge weights  $\alpha, \beta$  (top) and its proposed self-organizing circuit-based solution with edge memristors  $W^E$  and vertex memristors  $W^V$  (bottom).

Fig. 2 (top) shows a graph of two vertices  $A, B$  with two edge weights  $\alpha, \beta$ , respectively. Since memristors are directed electrical devices, it is possible to represent a directed graph in the circuit which is shown in Fig. 2 (bottom). Here,  $\alpha$  in series interconnected edge memristors  $W^E$  represent the weighted edge from  $B$  towards  $A$  while the series interconnection of  $\beta$  edge memristors  $W^E$  describes the weighted edge from  $A$  to  $B$ . The grounded vertex memristors  $W^V$  model the vertices  $A, B$ , respectively.

Below we will investigate a fundamental graph that will explain the roles of all involved memristors in detail.

### B. Fundamental Graph

Fig. 3 shows a fundamental directed graph with vertices  $A, B, C$  and three edges with edge weights of 1 each. This

graph is fundamental, because starting from entry vertex  $A$  there are two possible paths to vertex  $C$ . The path  $A \rightarrow B \rightarrow C$  has a cost of 2, while the path  $A \rightarrow C$  has a cost of 1 and is therefore optimal. The circuit corresponding to Fig. 3 is shown in Fig. 4.

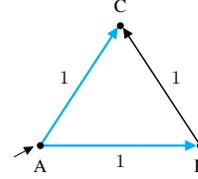


Fig. 3. Fundamental directed graph with entry vertex  $A$  marked by the arrow and optimal spanning tree indicated by blue edges.

All edge memristors are initialized in the LCS and all vertex memristors are initialized in the HCS, so that the initial inner states are  $z_0^E = 1$  and  $z_0^V = 0$ . This can be seen in Fig. 4 (a), where all LCS memristors are highlighted in orange and all HCS memristors are shown in blue. The goal of this setup is to have all edge memristors that are part of the minimal spanning tree to be in the HCS after convergence.

Due to the configuration depicted in Fig. 4 (a) and  $W_{LCS}^E \ll W_{HCS}^V$ , cf. (2),  $W_1^E$  and  $W_3^E$  observe almost the entire voltage  $u_{in} > 0$  while all other memristors experience close to no voltage at all. This will cause both  $W_1^E$  and  $W_3^E$  to transition to the HCS, which is shown in Fig. 4 (b) and indicates that both are part of the minimal spanning tree. In this new configuration, again due to (2), the two vertex memristors  $W_B^V$  and  $W_C^V$  will transition to the LCS, as the voltage across both is approximately  $-u_{in}$ . This leads to the final configuration that is shown in Fig. 4 (c), where all memristors in the HCS are part of the minimal spanning tree and all other memristors are in the LCS. Understanding this fundamental setup enables approaching graphs of arbitrary sizes and arbitrary, non-negative edge weights.

## III. WAVE DIGITAL MODEL

The wave digital concept [13] is here exploited as an emulation technique as it is known to yield a highly flexible algorithm where parametric changes and especially the incorporation of different memristor models is quick and uncomplicated [10], [11]. Additionally, energetic properties such as passivity are preserved and the resulting algorithm can be implemented on a DSP or a FPGA for real time applications in integrated circuits [12].

At an arbitrary port, electrical quantities  $u, i$  are related to wave quantities  $a, b$  by an arbitrary constant  $R > 0$  called the port resistance and the transformation

$$a = u + Ri, \quad b = u - Ri. \quad (3)$$

Any circuit solution to the here investigated problem like the one shown in Fig. 4 is a network consisting of multiple memristors that can always be expressed by a single one-port memristor  $\hat{W}(z, u)$  with a resistive voltage source as the input signal as explained in [1]. Such a compact representation

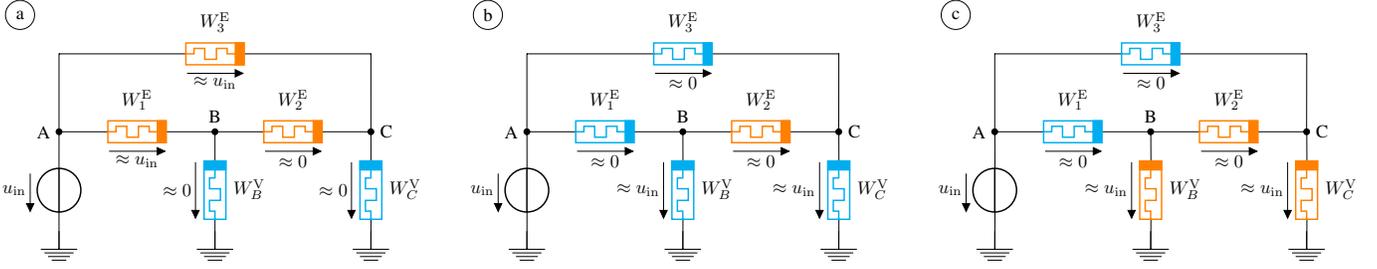


Fig. 4. Proposed circuit for the fundamental graph setup of Fig. 3. Understanding the processes of this setup is key to understand arbitrary setups. Memristors in LCS are highlighted in orange, those in HCS are highlighted in blue. Figures (a)-(c) show states and experienced voltages of all memristors until convergence. The problem solution can be observed from (c) where all edge memristors that are part of the minimal spanning tree are in the HCS.

highly simplifies the derivation of a signal flow graph with wave quantities which is shown in the following.

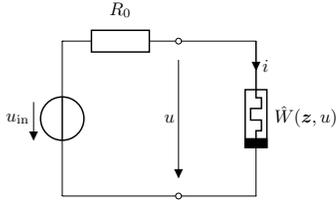


Fig. 5. Resistive voltage source with input  $u_{in}$  connected to memristor  $\hat{W}(z, u)$  which represents the memristive circuit solution to the minimal spanning tree problem.

The resistive voltage source in Fig. 5 is expressed in wave quantities by

$$u = e - R_0 i \Leftrightarrow a = e, \quad (4)$$

if the port resistance is chosen such that  $R = R_0$ . The memristor in Fig. 5 can be expressed as

$$i = \hat{W}(z, u) u \Leftrightarrow b = \rho(z, u) a, \quad (5)$$

where the reflection coefficient is

$$\rho(z, u) = \frac{1 - R_0 \hat{W}(z, u)}{1 + R_0 \hat{W}(z, u)}. \quad (6)$$

The overall wave digital signal flow graph is depicted in Fig. 6, where highlighted parametric loop is addressed by fix-point iterations [14].

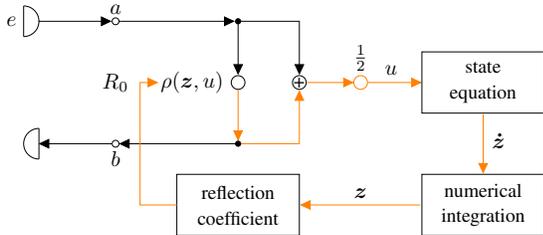


Fig. 6. Wave digital flow graph of the setup in Fig. 5 with the parametric loop highlighted in orange.

## IV. EMULATION RESULTS

Based on the functionality explained for the fundamental graph in Fig. 3, we investigate the course of the inner states for the edge memristors in Fig. 9 with the emulation parameters specified in Table I.

Emulation parameters			
$W_{LRS}^E$	= 1 kS	$u_0$	= 1 V
$W_{LRS}^V$	= 1 S	$T_{in}$	= 2 ms
$W_{HRS}^E$	= 1 mS	$R_0$	= $1 \mu\Omega$
$W_{HRS}^V$	= $1 \mu S$	$S$	= $10^3$

TABLE I

EMULATION PARAMETERS FOR THE SETUP DEPICTED IN FIG. 9 (BOTTOM).

The input signal is a train of rectangle pulses, which is designed such that one rectangle causes a single edge memristor  $M^E$  to transition from the LCS to HCS, cf. Fig. 8. This way the amount of rectangles needed coincides with the costs from the entry vertex to any other vertex. The emulation results are shown in Fig. IV.

Firstly, we observe that all memristors  $W_1^E, \dots, W_8^E$  that should be part of the minimum spanning tree are in the HCS after convergence as indicated by the course of their initial states  $z_1^E, \dots, z_8^E$ . The first memristor to transition from LCS to HCS is  $W_1^E$  after two rectangular inputs. Here, we see that the cost from vertex  $A$  to vertex  $B$  has indeed a cost of 2 which verifies the proper design of the input signal as depicted in Fig. 8. Only after  $W_1^E$  is in the HCS,  $W_2^E$  experiences the next rectangular input, causing it to go to the HCS since the cost from vertex  $B$  to vertex  $C$  is 1. With the fourth rectangular input,  $W_6^E$  transitions to the HCS, as the costs  $A \rightarrow G$  are 4. Note that both branches of the minimum spanning tree are found simultaneously and do not require overwriting previous states as for example in Dijkstra's algorithm [7]. Consequently, all other paths are found at a time proportional to their costs. From Fig. 8 it can be seen that the minimum spanning tree contains a path of length 19.

## V. CONCLUSION AND OUTLOOK

In this paper a circuit-based, self-organizing solution to the minimum spanning tree problem based on a memristive network has been investigated. Especially in large application

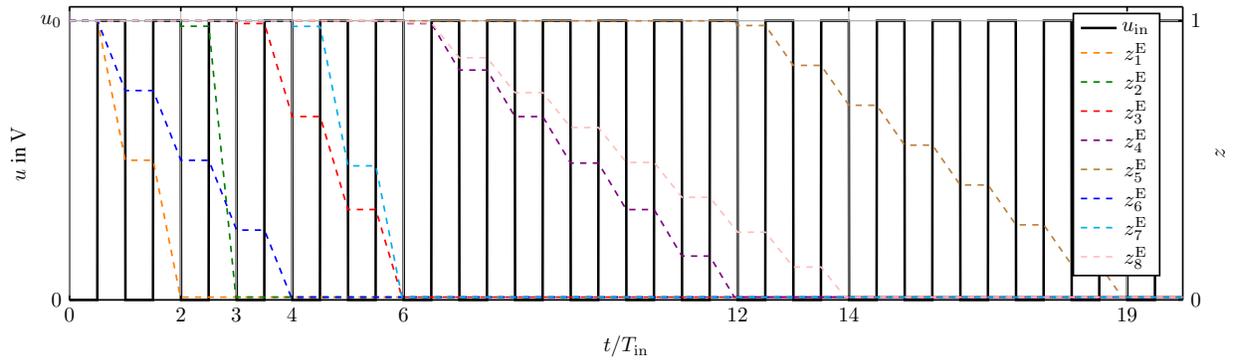


Fig. 8. Emulation results of states  $z_1^E, \dots, z_8^E$  in the setup shown in Fig. 9 when the signal  $u_{in}$  is applied as displayed. It can be observed that the according edge memristors transitions to the HCS when the number of spikes of the input signal  $u_{in}$  coincides with the costs from vertex A to the respective vertex.

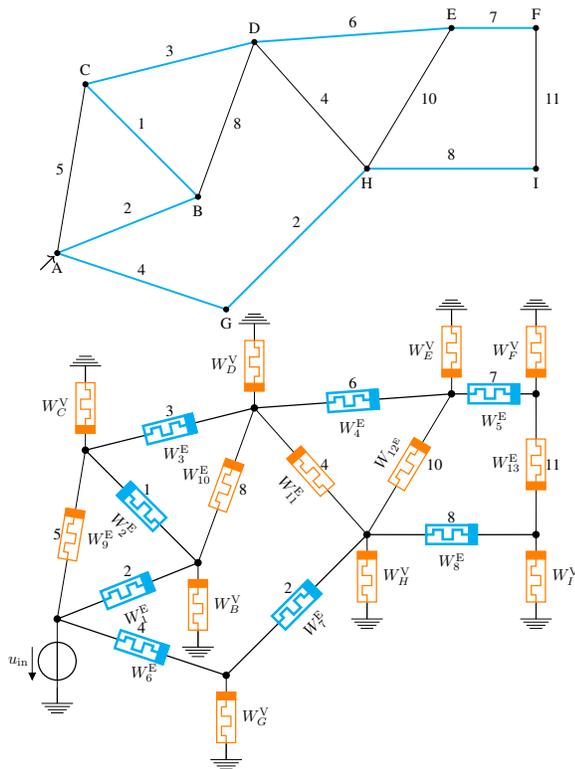


Fig. 9. Graph with entry vertex  $A$ , vertices  $B, \dots, I$  and edges  $1, \dots, 13$  with edge weights written next to them (top). Memristive circuit where the colors indicate the final solution of the problem with memristors in HCS are highlighted in blue and those in LCS highlighted in orange (bottom). Simulation results of this setup are shown in Fig. 8.

examples, such as neural networks, an approach that is able to organize itself like the one presented in this work are desirable because they might correspond to unsupervised topology formation and optimal information transmission. A highly flexible emulator based on wave digital principles has been provided and the concluding emulation results have verified a proper functioning of the proposed memristive circuit and the emulator thereof.

Models of physical memristors can easily be incorporated

in the here presented emulator for future work, making it a highly universal investigation tool and design aid.

#### ACKNOWLEDGMENT

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