Received 26 April 2016; | Revised 6 June 2016; | Accepted 6 June 2016

DOI: xxx/xxxx

RESEARCH ARTICLE

# Wave Digital Model of a TiN/Ti/$HfO_2$/TiN Memristor

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**Summary**

Memristors - nonlinear resistors with memory - are potential candidates for the utilization in self-organizing circuits. These novel elements need innovative technological developments in order to incorporate them into integrated electrical circuits. Alternatively, $HfO_2$-based resistive random access memories (RRAMs) are complementary metal-oxide-semiconductor (CMOS) compatible and can also be interpreted as memristive devices. A fingerprint of such devices is their rapid change between the high and low resistance state. It is intended to exploit this feature in self-organizing circuits to achieve a desired overall functionality. But the huge device variabilities exacerbate pre-investigations of real circuits including such devices. To this end, a wave digital model based on a mathematical as well as a physical model of a hafnium oxide ($HfO_2$) memristor is introduced. Utilizing the wave digital approach yields a flexible, real-time capable algorithmic model which is suitable for live parameter fitting in real circuits. Comparisons of the emulated hysteresis with measured data of RRAM cells verify the functionality of the presented emulator. The proposed method for emulating physical systems is not restricted to single devices. Indeed, whole sub-circuits can be emulated before fabrication in order to save development costs.

**KEYWORDS:**
memristive devices, resistive switching, wave digital filter, memristor emulators

## 1 | INTRODUCTION

An innovative approach for designing systems with self-organizing capabilities on a hardware level is to use circuit elements with memory. Self-organization in this manner means that the parameters of an electrical circuit can be adaptively adjusted in dependence of environmental influences. The memory effect increases the performance of such circuits because it introduces a kind of learning from environmental influences in the past. With this, the electrical circuits are not only reacting on instantaneous stimulus but consider also prior events in order to react more efficiently. Potential candidates among others with respect to this kind of applications are memristive devices [1,2]. Memristive devices or memristors are nonlinear resistors with memory, which are able to change their resistance/memristance depending on the stimulus. In contrast to general nonlinear resistors, memristors maintain the actual memristance value after extinguishing the applied excitation. Such devices have already been utilized in self-organizing circuits. A prominent example is a memristive circuit imitating amoeba learning [3,4]. Neuromorphic circuits based on memristors as synapses for coupling neurons are presented in [5,6,7]. Unfortunately, these devices are hard to fabricate and need a novel technology in order to incorporate them into integrated electrical circuits. RRAM cells can be a good choice, because these nonvolatile memories are in fact memristive devices [8]. In particular, $HfO_2$-based RRAM devices are CMOS compatible which let us exploit its maturity and low fabrication costs.

RRAM-based memristors exhibit a binary switching behavior, where the switching threshold varies due to fabrication inaccuracies. This device variability of RRAM cells[9,10,11] prevents a suitable designing process of electrical circuits to achieve a specified functionality. To overcome this problem, one can use appropriate emulators. This yields the possibility for an adequately designing process of electrical circuits including such devices. Efficient memristive hardware emulators have already been introduced[12,13,14,15]. Those emulators consist of active circuit elements with a fixed functionality. Especially regarding the device variability of RRAM cells, a more flexible emulator is desired in order to make investigations with respect to some parameter spread within the emulator. To this end, in the presented paper an emulator of a $HfO_2$ RRAM cell based on wave digital principles[16] is introduced. The wave digital approach mainly transforms an analog reference circuit into an algorithmic model which is real-time capable while maintaining the energetic properties of the underlying analog circuit[17]. The main benefit of the wave digital approach in the context of memristor emulators is its flexibility[18,19,20]. Since the resulting algorithmic model can be implemented platform independent, reconfigurable emulators with the possibility for changing parameters during runtime can be achieved[21]. With this, live parameter fitting can be done in order to figure out suitable parameters for a desired overall functionality of circuits including such devices. Moreover, whole sub-circuits instead of single devices can be emulated by the proposed method[22,23].

A combined physical and mathematical model is utilized in order to get a reference circuit of the RRAM cell, which in turn can be transformed into the wave digital domain. The high and low resistance states of the device are modeled physically more accurate based on the QPC (quantum point contact) theory[24,25,26], whereas the switching behavior is incorporated mathematically but still with physically interpretable parameters. This method is reasonable because the switching behavior itself varies stochastically and is a very fast procedure. The semi-physical model in combination with the wave digital approach yields a very efficient, robust and flexible emulator for the utilization in real-time applications.

Subsequently, a physical description of the $HfO_2$-based RRAM cell is recapitulated. Based on these insights, the QPC-theory is applied in order to get a physical model for the high as well as low resistance state of the device. Those models are interpreted in an electrical manner for a wave digital realization. Afterwards, the switching behavior of the device is modeled mathematically in order to connect the two distinct states together. With this, a reference circuit is determined which is exploited to get the wave digital algorithmic model. Emulation results are shown by inspecting the hysteresis curve and compare it with measured data. Main results of the proposed paper are summarized in the conclusion at the end of the manuscript.

## 2 | PHYSICAL DESCRIPTION

The investigated memristor consists of a TiN/Ti/$HfO_2$/TiN (titanium nitride/titanium/hafnium oxide/titanium nitride) structure. In this composition the top as well as the bottom electrode of the resistive switching device are composed of titanium nitride. Hafnium oxide is the dielectric layer often called as the memristive layer in the context of memristive devices and systems[27]. The proposed structure includes a thin titanium layer between the top electrode and the dielectric. This thin film of titanium acts as a getter material for oxygen ions and supports the forming of a conductive filament within the dielectric[25]. Applying a positive voltage yields a movement of negative oxygen ions into the titanium layer and simultaneously to a higher concentration of positive oxygen vacancies in the dielectric layer, which in turn forms the conductive filament profile between top and bottom electrode, cf. Fig. 1 . Since the investigated resistive switching device belongs to the class of bipolar switching devices, a conversion of the applied voltage yields to a gap within the filament. This forming and rupture of the conductive filament defines the low and high resistance state of the device, respectively. The transition from the high resistance state to the low resistance state is also called the set process, whereas the opposite transition is described by the reset process.

The initial forming process of the conductive filament in the $HfO_2$ layer occurs during the fabrication of such devices. Describing the internal physical and chemical phenomena during this procedure needs a more detailed modeling approach. We want to model such devices with respect to emulation purposes in order to incorporate them into real circuits. Hence, neglecting the forming procedure in the proposed modeling approach is reasonable. To this end and according to the results presented in[25,24,26], the quantum point contact (QPC) theory is used in our modeling approach in order to explain the electron transport mechanism in $HfO_2$-based resistive random access devices. The QPC theory provides an expression for the current through the conducting filament between two electrodes based on the Landauer transmission approach[24]

$$i(t) = \frac{2e}{h} N \left[ eu(t) + \frac{1}{\alpha} \ln \left( \frac{1 + \mathrm{e}^{\alpha[\Phi - \beta eu(t)]}}{1 + \mathrm{e}^{\alpha[\Phi + [1-\beta] eu(t)]}} \right) \right] , \tag{1}$$

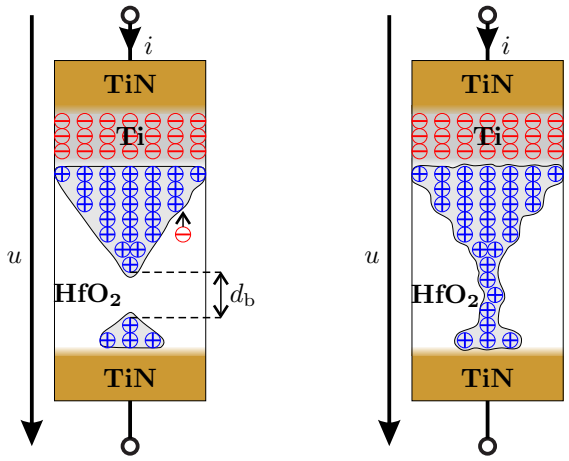


**FIGURE 1** Illustrative sketch of the device and internal states with respect to the high resistance state on the left-hand side and to the low resistance state on the right-hand side. Here, $d_\mathrm{b}$ denotes the gap in the conducting filaments, which is $d_\mathrm{b} > 0$ in the high resistance state and $d_\mathrm{b} = 0$ in the low resistance state, respectively.

where $e$ and $h$ are the electron charge and Planck constant, and $u(t)$ denotes the applied voltage to the device, which is assumed to drop at the cathode and anode interfaces in a fraction of $\beta$ and $[1-\beta]$. Equation 1 results from the transmission probability of electrons when assuming an inverted parabolic potential barrier[25], where $\Phi$ is the barrier height and $\alpha$ is related to the inverse of potential barrier curvature. It is also possible that there is more than a single conductive filament, $N$ in number, contributing to the overall current flow through the switching layer. Referring to[26], we assume in the proposed modeling approach the possibility of having multiple conductive filaments in the low resistance state (LRS) and a single tunneling path in the high resistance state (HRS). With this, the approximations

$$i_\mathrm{LRS}(t) = \frac{2e^2}{h} N u(t) \quad \text{and} \quad i_\mathrm{HRS}(t) = \frac{2e}{h}\left[eu(t) + \frac{1}{\alpha}\ln\left(\frac{1+\mathrm{e}^{\alpha[\Phi-\beta eu(t)]}}{1+\mathrm{e}^{\alpha[\Phi+[1-\beta]eu(t)]}}\right)\right] \tag{2}$$

depending on $\Phi$ and $\alpha$ for the two distinct states are expedient. The QPC model is in particular beneficial for the modeling of such devices in an electrical manner because of the analytical expressions for the resulting current, which can be directly interpreted as an electrical one-port. Based on the QPC theory an electrical model of the device including a switching behavior is shown in the next section.

## 3 | ELECTRICAL MODEL

An electrical representation of the device consisting of lumped elements is a necessary requirement in order to get a wave digital emulator. In the context of wave digital filters, such models are referred to as reference circuits. As an example, in[27] the procedure starting from a physical description of a memristive device up to a concentrated model is shown in detail.

The recapitulated QPC theory describes the current through the device for the low as well as high resistance state. The latter can be interpreted as a nonlinear resistor, whereas in the low resistance state the expression in Equation 2 describes a linear resistor. We intended to introduce two electrical one-ports representing the low and high resistance states, respectively. Therefore, the equations for the current are reformulated in terms of linear and nonlinear resistances in order to achieve an electrical equivalent circuit. In this context, the low resistance state is described by a linear resistor

$$R_0 = \frac{1}{N G_\mathrm{q}}, \quad \text{with} \quad G_\mathrm{q} = \frac{i_0}{u_0}, \quad i_0 = \frac{2e}{h\alpha}, \quad \text{and} \quad u_0 = \frac{1}{e\alpha}, \tag{3}$$

with the quantum conductance unit $G_\mathrm{q}$, a normalization current $i_0$ and voltage $u_0$. In contrast to the low resistance state, the corresponding resistor with respect to the high resistance state is nonlinear describing the tunneling of electrons through a

potential barrier

$$R_1(u) = \frac{u}{G_q u + i_0 \ln\left(\frac{1+e^{\gamma-\beta u/u_0}}{1+e^{\gamma+[1-\beta]u/u_0}}\right)}\,, \tag{4}$$

with $\gamma = \alpha\Phi$ as a material parameter. In the case of small voltages, this nonlinear expression can be approximated by a linear one

$$\lim_{u\to 0} R_1(u) = R_q\left[1+e^{\gamma}\right]\,, \quad \text{with} \quad R_q = \frac{1}{G_q}\,. \tag{5}$$

The corresponding electrical one-ports are depicted in Fig. 2 .

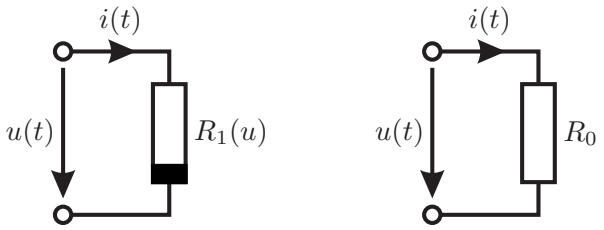


**FIGURE 2** Electrical representation of the high (left) as well as low (right) resistance states of the RRAM cell.

## 3.1 | Electrical Interpretation of the Internal State

Thus far the linkage between high and low resistance state is not considered. This linkage is important in order to incorporate the memory feature into the device description and also to classify the proposed device as a memristor. In the introduced modeling approach, this linkage should be created through an appropriately defined internal state. For that reason, the gap width in the conducting filament is interpreted as an internal state of the device

$$z = \frac{d_b}{D_0}\,, \quad 0 \le z \le 1\,, \tag{6}$$

with $D_0$ as a normalization width in order to restrict the internal state between 0 and 1. The QPC model in combination with this internal state defines a general memristor[2,8]

$$u(t) = R(z,u)\, i(t)\,, \quad \text{with} \quad R(z,u) = R_0 + z\left[R_1(u) - R_0\right] \quad \text{and} \quad \dot{z} = f(z,u)\,, \tag{7}$$

where the memristance $R$ depends on the applied voltage and changes linearly between the high and low resistance state with respect to the internal state $z$. The function $f$ is the so-called memristive function[28], which describes the change of the internal state depending on the actual state and the applied voltage.

Resistive switching devices implicate a huge device variability, in particular regarding the switching behavior[9,10]. Considering a physically accurate formulation for the memristive function $f$ needs a deeper modeling approach. In this work, the focus is on an as simple as possible model describing the behavior of resistive switching devices for the utilization as an emulator in real electrical circuits. In this context, the memristive function is modeled rather in a mathematical manner than in a physical one, which leads to a semi-physical overall model. Indeed, we assume a binary switching phenomenon between the high $z = 1$ and the low resistance state $z = 0$. The exploited model for the memristive function is inspired from[3] and exhibits an abrupt change considering the set process

$$\dot{z} = g(u)\left[\sigma(u)\,\sigma(z) + \sigma(-u)\,\sigma(1-z)\right]\,, \qquad \text{with} \qquad \sigma(\xi) = \begin{cases} 1\,, & \text{for} \quad \xi \ge 0 \\ 0\,, & \text{for} \quad \xi < 0 \end{cases}\,, \tag{8}$$

$$g(u) = S_p \Sigma\left(u - U_p\right) + S_n \Sigma\left(u - U_n\right)\,, \qquad \text{and} \qquad \Sigma(\xi) = \int_{-\infty}^{\xi} \sigma(\eta)\,\mathrm{d}\eta\,. \tag{9}$$

Here, $U_p$ and $U_n$ denote the threshold voltages for positive and negative bias, respectively. This means that the device starts changing its resistance above/below $U_p$/$U_n$, respectively, which is related to the set and reset process. The changing rate $g(u)$

including these parameters is illustrated in Fig. 3 (left). Corresponding slopes of the changing rate are denoted as $S_n$ and $S_p$. It is

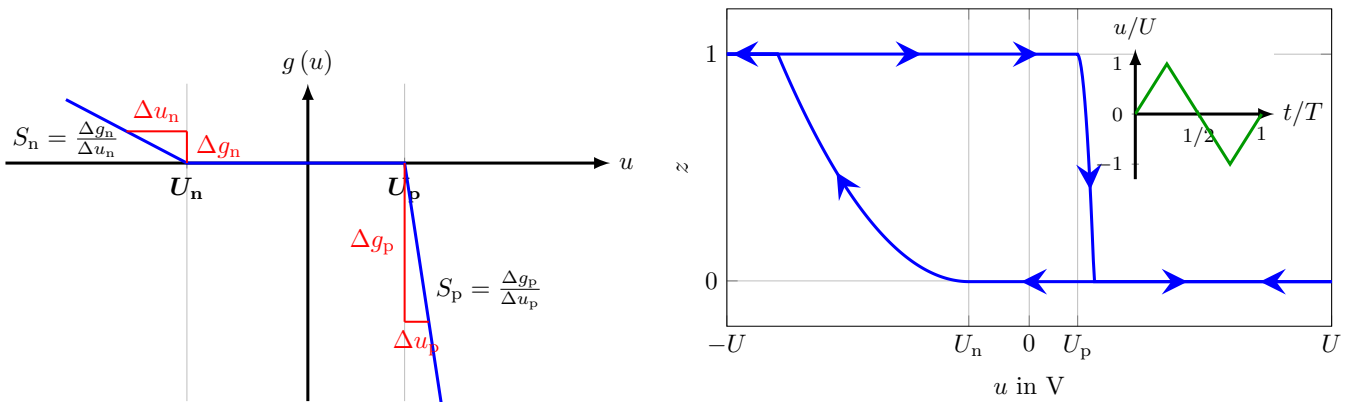


**FIGURE 3** Left: changing rate $g(u)$ with positive (set) and negative (reset) threshold voltages $U_p$ and $U_n$, respectively. The slopes for the changing rate with respect to the set and reset process are denoted by $S_p$ and $S_n$. Right: change of the state with respect to a triangular input voltage.

shown that for resistive switching devices based on conductive filaments, the set process is much faster than the reset process and also that the required voltage for the reset process is higher than the one regarding the set process which is in good coincidence with measured data as shown later in the manuscript. As an illustrative example, the state vs. voltage map is shown in Fig. 3 (right) with respect to a triangular input voltage (inset). Starting from a high resistance state $z = 1$ as an initial condition, the state rapidly decreases to the low resistance state $z = 0$ when the applied voltage crosses the threshold voltage $U_p$ for the set process. Consequently, as soon as the amplitude of the applied voltage reaches the threshold voltage $U_n$, which is related to the reset process, the internal state gradually changes from the low to the high resistance state. Although there is a very slow change of the internal state for voltages $U_n < u < U_p$ regarding real $HfO_2$ devices, in the proposed model this change is neglected. However this should be considered depending on the application and the applied input signal. Moreover the assumed changing rates $S_n$ and $S_p$ have been fitted to the measured data. It should be emphasized that those parameters also have to be optimized for different applied input signals. The overall memristive one-port with the corresponding equivalent circuit is shown in Fig. 4 .

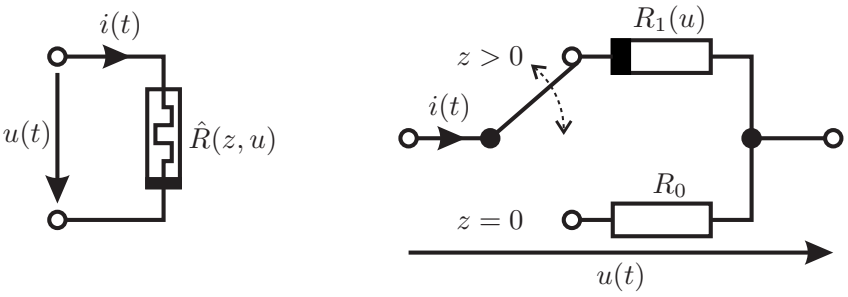


**FIGURE 4** Memristive one-port (left) and corresponding electrical interpretation of the internal state (right).

Although there is a parasitic memory impedance behavior of metal-insulator-metal structures[29], which are the dominating effects regarding higher frequency applications, it has been neglected in the proposed model. This is reasonable because the interesting feature considering information storage or neuromorphic operations is the threshold-dependent switching behavior. This feature is sufficiently covered by the presented model.

## $HfO_2$-Based Memristor

The $HfO_2$-based memristor is integrated in a 1T-1R memory cell[30]. These 1T-1R memory cells are constituted by a select nMOS transistor manufactured in BiCMOS technology (width of 1.14 µm and length of 0.24 µm), which also sets the current compliance, whose drain is in series to the memristive device. The memristive cell, which area is equal to 0.4 $\mu m^2$, consist of a metal-insulator-metal (MIM) structure. It is integrated on the metal line 2 of the BiCMOS process and composed by 150 nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 7 nm Ti layer, and an 8 nm $HfO_2$ layer deposited by atomic layer deposition (ALD). The schematic and cross-sectional TEM images of the integrated RRAM cell including the metal lines, the MIM materials, and the Tungsten-based via connections are shown in Fig. 5 .

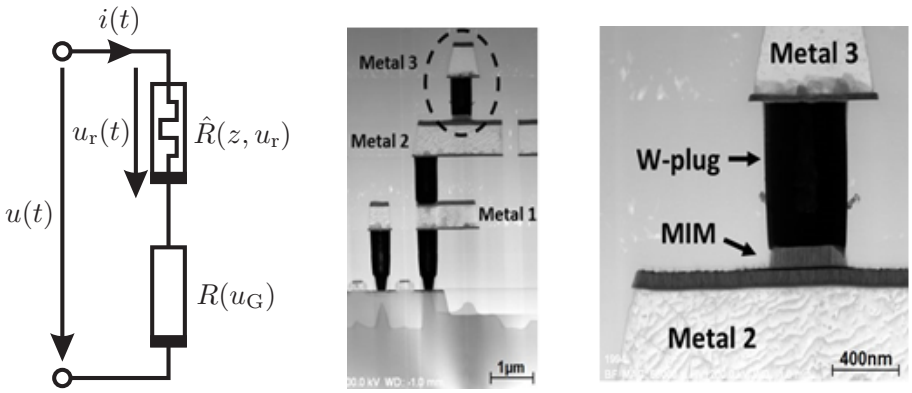


**FIGURE 5** Left: Resulting reference circuit of the memory cell. Middle: cross-sectional TEM image of the cell. Right: MIM stack insight.

In the reference circuit of the memory cell, the nMOS transistor is replaced by a parametric resistor, cf. Fig. 5 (left). The parameter $u_\mathrm{G}$ represents the gate voltage of the transistor, which controls the resistance, and hence the current compliance. According to that, for different values of the parameter $u_\mathrm{G}$ different current compliance levels can be achieved. This is especially beneficial in order to get a multilevel device, which can store intermediate states among the high and low resistance states. Since the transistor is responsible only for the described current compliance without significance considering the functionality of the memristive device, a more accurate model of the transistor would unnecessarily complicate the emulator. The overall reference circuit of the integrated memristive device is shown in Fig. 5 (left) and is utilized in the following as a reference circuit for the wave digital model.

The electrical characterization of the 1T-1R cells was performed in the DC mode. The applied voltage to the cell, which is the potential at the drain terminal, was raised from 0 V to 5 V during the set operation with $u_\mathrm{G} = 1.5$ V. Accordingly, it was decreased from 0 to −5 V during the reset procedure. A sweep ramp of 1 V/s was used, which leads to the triangular waveform shown in the inset of Fig. 3 (right). The DC-characteristics of 15 representative 1T-1R devices are illustrated in Fig. 6 .

## Spice Simulation

The introduced electrical model of the RRAM cell has been implemented in LTspice in order to compare the resulting hysteresis with measured data of the device. Measured parameters of the physical device are used in the model with minor modifications in order to fit the average measured hysteresis. Model parameters are listed in table A1 at the and of the manuscript. Simulated and measured hysteresis curves are shown in Fig. 7 . In contrast to Fig. 6 , in Fig. 7 the hysteresis is depicted on a logarithmic scale. This provides the comparison of measured data with simulated.

The QPC model assumes the existence of a filamentary path across the $HfO_2$ film. At its narrowest point, the first quantized band behaves like a potential barrier for the incoming electrons. The height of the potential barrier is determined by the cross-sectional area of the constriction and defines the two conduction states. However, the transitions between the two conduction states are not covered by the QPC model. Therefore the validity region of the QPC model is limited to typical read-out voltages below 0.5 V. In particular the good coincidence between measured and simulated data in the QPC-region is remarkable. After the set transition, when the device is switched into the low resistance state, the drop of voltage in the transistor is significantly

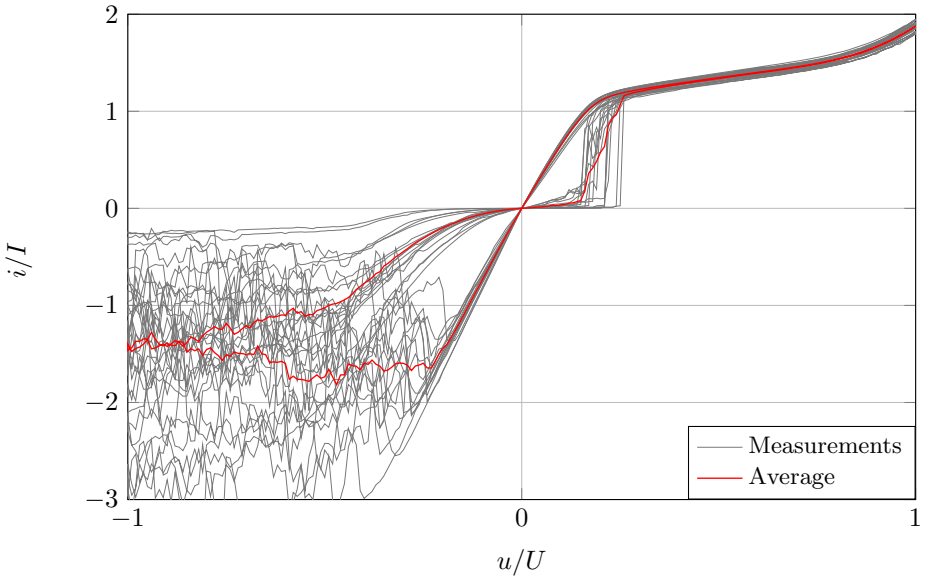


**FIGURE 6** DC-characteristics of 15 representative 1T-1R devices (grey lines) with normalization current $I = 20\ \mu A$. The red line illustrates the mean current values.

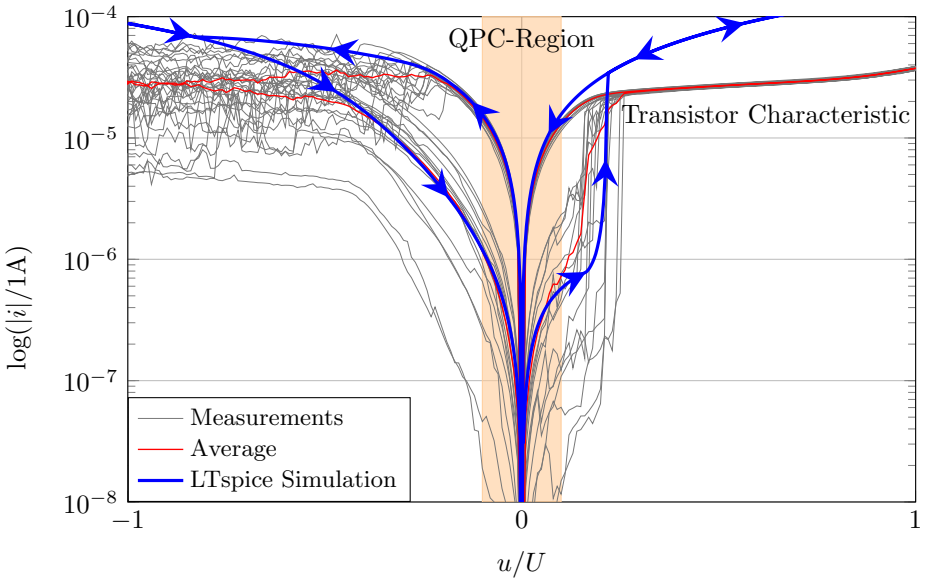


**FIGURE 7** Simulated hysteresis curve of the RRAM cell.

higher than before. Since the transistor has been replaced by a parametric resistor in the model, the discrepancies in these regions are more obvious. Nevertheless, the model is suitable to obtain pre-investigations in simulations of more complex memristive circuits regarding the more significant switching region.

## 4 | WAVE DIGITAL EMULATION

Low fabrication costs and CMOS compatibility make $HfO_2$-based memristors highly attractive candidates for the utilization in integrated self-organizing circuits[5,6,7]. Inherently available device variabilities of such devices[9] adversely affect pre-investigations of complex circuits including them. In this sense, mathematical or electrical models for uses in simulations are more appropriate. The equivalent circuit proposed in the previous section in combination with common circuit simulation tools is suitable for this purpose, as shown in the previous section. These simulations can support pre-examinations of memristive circuits before fabrication. With increasing complexity of memristive devices and circuits, the efficiency of such simulations decreases[31]. In our approach, we intended to use memristive emulators, which can be incorporated into real circuits in order to overcome the described problem. The crucial difference between a simulation and an emulation appears in the fact, that an emulation processes data streams in real-time, whereas in simulations ensembles of data blocks are processed. Efficient hardware emulators have already been presented. Most of them are based on active circuits consisting of operational amplifiers[13,14,15] which aggravates stability investigations of circuits including such emulators. In[12], a simple passive memristor emulator for research purposes is suggested. However, it should be emphasized that the proposed emulator is restricted regarding the functionality. A flexible memristor emulator with appropriate stability properties would be desirable in this context. These requirements concerning memristive emulators can be achieved by using the wave digital method[16,17]. The wave digital approach transforms the continuous model of a physical system represented by a reference circuit into a discrete model using wave quantities as signal parameters instead of voltages and currents. It yields a wave flow diagram of a physical system for platform-independent implementations, like on an ASIC (application specific integrated circuit) in order to get a hard-wired hardware emulator or on an FPGA (field programmable gate array) for a reconfigurable emulator. During this transformation, the energetic properties of the original continuous model are preserved[17], which in particular means that passivity is maintained in a digital signal processing sense. More precisely, wave quantities in combination with a passive integration method regarding reactive elements in the discrete model preserves the passivity property of the underlying passive circuit. Since the memristance value is positive independent of the internal state, passivity for memristive ports are ensured in the wave domain. Moreover, the introduction of wave quantities leads to a port-wise evaluation of the passivity, even under finite arithmetic conditions. A general approach for wave digital emulators of memristive devices is introduced in[19,20,28]. The main benefit, among others, of emulators based on wave digital principles, is the flexibility, which is manifested in two different ways: the flexibility of implementation the resulting algorithmic model on different platforms and the flexibility of the utilized memristive model itself. In Addition, the parameters of the model can be adjusted during runtime, which leads to the possibility of live parameter fitting[21]. With this, the device variability of RRAM cells can be adequately modeled in order to investigate the influence on the functionality of the overall circuit[18]. Regarding all these arguments, the wave digital model of the $HfO_2$-based memristive device is introduced in the following.

The wave digital approach uses wave quantities as signal parameters instead of voltages and currents. Both domains are linked through a bijective mapping

$$a = u + R\,i \quad \text{and} \quad b = u - R\,i\,, \quad \text{with} \quad R > 0\,. \tag{10}$$

Here, $a$ and $b$ denote the incident and reflected waves at a particular port, respectively. The positive parameter $R$ is the port resistance, which is known from scattering parameter theory. Another benefit of the wave digital approach is the modularity of the concept. For this, the underlying reference circuit, representing the physical system for emulation, has to be decomposed port-wise into electrical devices and into a Kirchhoff interconnection network connecting the devices together. Modularity in this context means, that all of these parts can be transformed into the wave domain independently in order to recombine them after the transformation to an overall wave digital structure. In the following the wave digital model of the $HfO_2$-based memristor is introduced. To this end, the emulation scenario is shown in Fig. 8 . On the left-hand side of Fig. 8 the equivalent circuit of the integrated RRAM cell is shown, cf. Fig 5 , whereas on the right-hand side an integrator circuit for an electrical interpretation of the internal state is depicted. In order to verify the emulated model, it is directly coupled to a resistive voltage source which generates the input signal.

Since the resulting wave digital algorithmic model processes data in a digital signal processing sense, the underlying system equations have to be discretized. Therefore, we introduce instances of time $t_k = t_0 + k\,T$, with $k \in \mathbb{N}$, starting time $t_0$ and sampling period $T$. Especially regarding memristive devices and systems this discretization leads to a numerical integration of

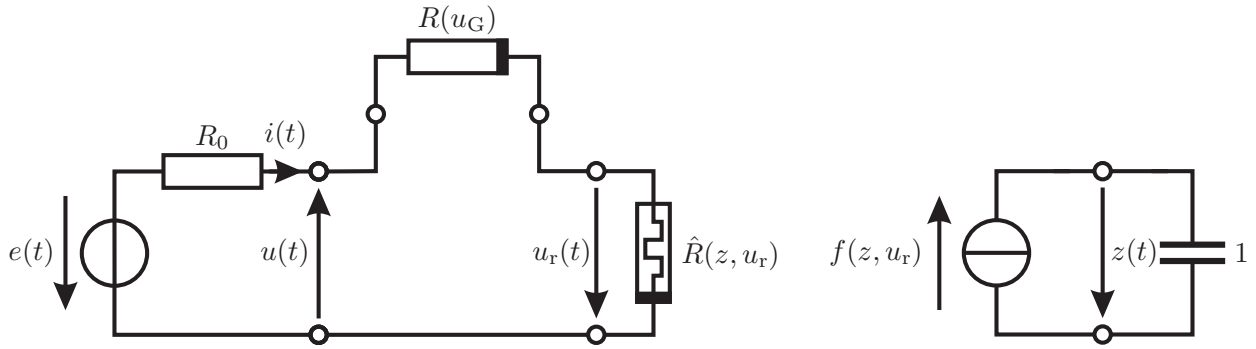


**FIGURE 8** Emulation scenario based on experimental measurements of the integrated device and integrator circuit representing the internal state.

the state equation, cf. Equation 7. Since the trapezoidal rule

$$z(t) = z(t_0) + \int_{t0}^{t} z(\tau)\,\mathrm{d}\tau \qquad\qquad z(t_k) \approx z(t_{k-1}) + \frac{T}{2}\left[z(t_k) + z(t_{k-1})\right] \tag{11}$$

is a passive integration method[32], it is commonly utilized in the context of wave digital models[17]. With this numerical integration of the state equation, the input-output relation can be modeled by a reflection coefficient, which depends on the actual memristance value

$$u_r(t) = \hat{R}\left(z, u_r\right)\, i(t) \qquad\qquad b(t_k) = \hat{\rho}\left(z, u_r\right)\, a(t_k)\,, \quad \text{with} \quad \hat{\rho}\left(z, u_r\right) = \frac{\hat{R}\left(z, u_r\right) - R_3}{\hat{R}\left(z, u_r\right) + R_3}\,. \tag{12}$$

In the proposed emulation scenario $R_3$ denotes the port resistance corresponding to the memristive port. A more general approach for the wave digital modeling of memristive systems is introduced in[28] with examples considering mathematical as well as physical models of memristors. The nonlinear resistor can also be modeled by a reflection coefficient

$$\rho(u_G) = \frac{R\left(u_G\right) - R_2}{R\left(u_G\right) - R_2}\,, \tag{13}$$

but in contrast to memristive wave digital models, the nonlinear resistor is defined by a pure algebraic equation. The wave digital representation of the algebraic input-output equation and the related model of the state equation is shown in Fig. 9 . The remaining series interconnection is depicted as a series adaptor. In order to avoid unnecessary structural delay-free loops

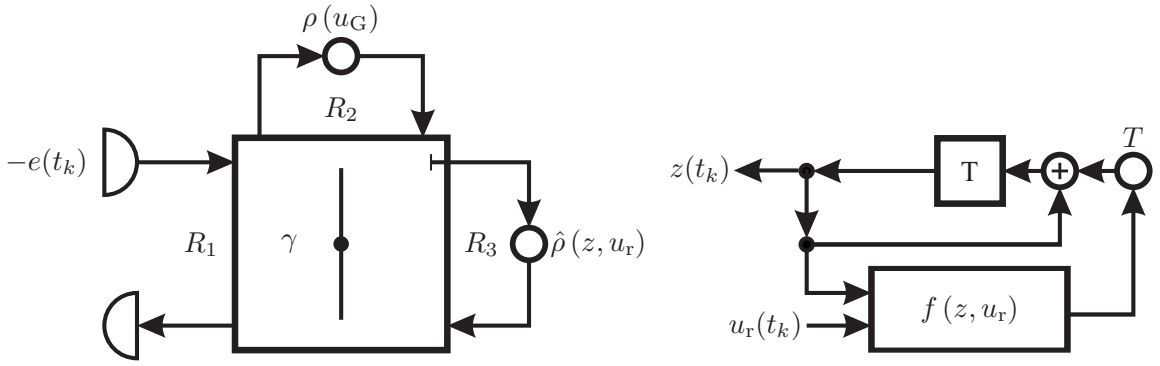


**FIGURE 9** Wave digital structure of the emulation scenario.

in the wave flow diagram and to get numerically convenient multiplier coefficients, the port resistances at the series adaptor are particularly chosen with $R_1 = R_0$ and $R_2 = \left(\max\left(R\left(u_G\right)\right) - \min\left(R\left(u_G\right)\right)\right)/2$, with adaptor coefficient $\gamma = R_1/R_3$, and

$R_3 = R_1 + R_2$, if port 3 is chosen to be reflection-free. A detailed explanation of the wave digital method would be beyond the scope of the proposed paper. All details about the wave digital modeling approach can be found in [16,17]. However, dealing with memristive devices in the wave digital domain is not comparable to nonlinear devices which lead to topology-related delay-free loops in the signal flow diagram[33]. Since memristors include an internal state, which depends on external signals, differential-algebraic delay-free loops occur[28]. In order to solve these implicit equations, a structurally modular and easy to implement fixed-point iteration scheme is exploited. Depending on different applications, the proposed method can be replaced by other iteration methods regarding convergence properties. The implementation overhead with respect to other iteration methods was not necessary for the underlying model.

## Emulation Results

The wave digital emulation result is shown in Fig. 10 . There, the hysteresis curves of measured and emulated devices are

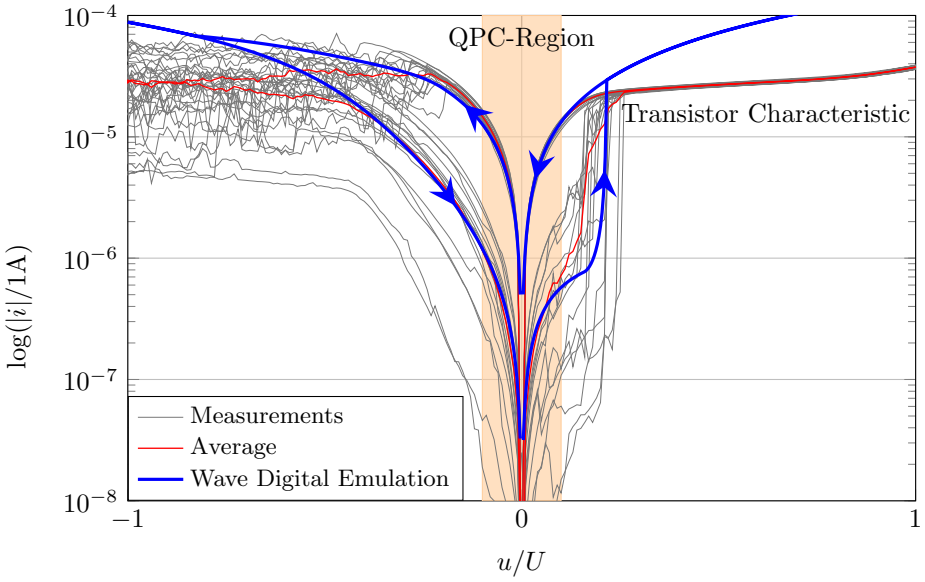


**FIGURE 10** Emulated hysteresis curve of the RRAM cell.

depicted. As mentioned before, the device variability corresponding to the set and reset process can be obtained by different measured curves. However, the good coincidence of the emulated and the average measured hysteresis is remarkable. A different background color has been utilized in order to emphasize the region where the QPC model is valid. This region should be considered when using the algorithmic model in optimization applications for parameter fitting. In particular, the wave digital algorithm is suitable in the context of optimization frameworks to figure out optimal model parameters with respect to measurements. A similar approach, where the wave digital model of a double barrier memristive device has been exploited to figure out a justified model reduction has already been introduced[21]. For higher voltage regions, the device changes from the high resistance state into the low resistance state and therefore the current-voltage relation is given by the transistor in series. This is also the reason for the discrepancies between emulated and measured hysteresis in these regions. The characteristic curve of the transistor distinguishes from that of the parametric resistor.

In order to verify the multilevel capability of the wave digital emulator, the series resistance value representing the transistor has been assumed to be normally distributed with mean value $R(u_\mathrm{G}) = 32\ \mathrm{k\Omega}$ and variance $100\ \Omega$. The resulting hysteresis curves for positive applied voltages are depicted in Fig. 11 . Resulting maximum, minimum and mean current values are coded by a blue, red, and black color, respectively. As can be seen, the device can be used for the storage of more than two distinct states and therefore more information can be represented. Especially, regarding neuromorphic circuits, intermediate synaptic coupling strengths are desired, which can be achieved by the multilevel characteristic of the RRAM cell.

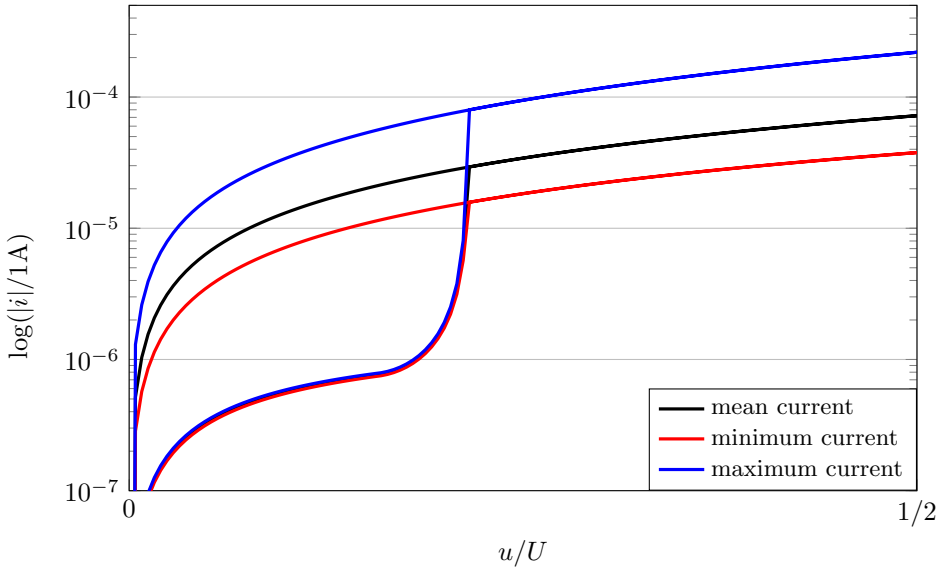


**FIGURE 11** Multilevel characteristic of the wave digital emulator with respect to different series resistances depending on the applied gate voltage $u_G$. Resulting maximum current values are shown in blue, minimum current values in red, and the mean value is shown in black color, respectively.

## 5 | CONCLUSION

In conclusion, the wave digital emulator of a $HfO_2$-based memristor has been introduced. CMOS compatibility of such devices makes them appropriate candidates for future technologies regarding self-organizing electrical circuits. The emulator is based on a mathematical as well as physical model by applying the QPC theory for describing the high and low resistance states of the device separately and by introducing a mathematical description for the switching behavior. A suitable interpretation of the internal state as a gap in conducting filaments within the device yields to a memristive model described by an input-output and a state equation. With the proposed approach, the high variability of RRAM cells can be emulated adequately in order to make pre-investigations with circuits including such devices. The high flexibility of the wave digital approach enables live parameter fitting of the proposed memristor in real circuits. A good coincidence between the emulated and measured hysteresis curve verifies the wave digital model of the memristive device. A parametric resistor has been used for current compliance, which is replaced by a transistor in the real device. With this, more than two distinct states can be stored within the device, which makes the proposed RRAM cell more suitable for neuromorphic applications.

It should be emphasized that the proposed emulation technique is not restricted to a single device. Instead of a single device, a whole sub-circuit of a real circuit can be emulated with the wave digital concept. With this, parameter optimization or a live parameter fitting with respect to a desired overall functionality of a circuit can be done. Whole circuits and single devices can be examined before fabrication which is quite important from an economic point of view.

## ACKNOWLEDGMENTS

The financial support by the German Research Foundation (Deutsche Forschungsgemeinschaft - DFG) through FOR 2093 and through DFG project number 404291403 is gratefully acknowledged.

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**How to cite this article:** E. Solan, and K. Ochs (2018), Wave Digital Model of a TiN/Ti/$HfO_2$/TiN Memristor, *Q.J.R. Meteorol. Soc.*, *2017;00:1–6*.

# APPENDIX

## A TABLES

**TABLE A1** $HfO_2$-based RRAM cell

| | | |
|---|---|---|
| Physical Parameters | | |
| Potential barrier | $\Phi = 1.9$ | eV |
| Inverse potential barrier curvature | $\alpha = 2$ | $1/$ [eV] |
| Amount of voltage drop top electrode | $\beta = 0.1$ | |
| Number of vacancy paths | $N = 1.5$ | |
| Electrical Parameters | | |
| Slope of the changing rate for positive bias | $S_p = -50$ | Hz/V |
| Slope of the changing rate for negative bias | $S_n = -0.4$ | Hz/V |
| Threshold voltage for the set process | $U_p = 0.8$ | V |
| Threshold voltage for the reset process | $U_n = -1$ | V |